

## PATENT ABSTRACTS OF JAPAN

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(71)Applicant : TOKUYAMA SODA CO LTD  
 (72)Inventor : ITO JUNICHI  
 SHIMAMOTO TOSHIJI

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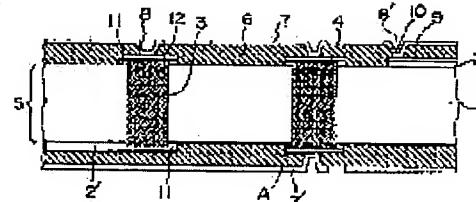
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**(54) MULTILAYER CIRCUIT BOARD AND MANUFACTURE THEREOF**

**(57)Abstract:**

**PURPOSE:** To keep laminated circuit patterns high in electrical connection reliability between them.

**CONSTITUTION:** First circuit patterns 2 and 2' are formed on the upside and underside of an insulating board 1, a conductive material 4 is filled into a through-hole 3 bored in the insulating board 1, and a through-hole section A is provided for the formation of a double-sided circuit board 5 whose surfaces are even, wherein the end faces of the conductive material 4 are nearly flush with the surfaces of the first circuit patterns 2 and 2' respectively. Second circuit patterns 7 and 7' of plating layer are formed on the both sides of the double-sided circuit board 5 through the intermediary of an insulating layer 6 respectively. The second circuit patterns 7 and 7' and the through-hole section A are electrically connected together with a solid plating layer 10, and the first circuit patterns 2 and 2' and the second circuit patterns 7 and 7' are connected together also with the solid plating layer 10.



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## CLAIMS

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## [Claim(s)]

[Claim 1]A breakthrough which has the 1st layer circuit pattern provided in both sides of an insulating substrate, and penetrates an insulating substrate is filled up with a conductive substance, . Have the through hole part formed so that the end face of this packing might turn into the surface of this 1st layer circuit pattern at the same flat surface mostly. It is a multilayered circuit board including the 2nd layer circuit pattern that consists of a metal skin by which the surface was established in at least one surface of a flat double-sided circuit board and this double-sided circuit board via an insulating layer, An electrical link between this 2nd layer circuit pattern and this through hole part, A multilayered circuit board accomplished by forming an opening in this insulating layer and covering an exposed part of a wall of this opening, and the end face of said through hole part with a metal skin of the 2nd layer circuit pattern, and a continuous metal skin so that at least a part of end face of this through hole part may be exposed.

[Claim 2]A breakthrough which has the 1st layer circuit pattern provided in both sides of an insulating substrate, and penetrates an insulating substrate is filled up with a conductive substance, The surface which has the through hole part formed so that the end face of this packing might turn into the surface of this 1st layer circuit pattern at the same flat surface mostly produces a flat double-sided circuit board, An insulating layer in which an opening was formed so that at least a part of end face of this through hole part might be exposed on at least one surface of this double-sided circuit board is provided, A manufacturing method of a multilayered circuit board which consists of covering an exposed part of the end face of a wall of an outside surface of this insulating layer, and this opening, said through hole, etc. with a continuous metal skin, etching a prescribed spot of this metal skin, and forming the 2nd layer circuit pattern.

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## DETAILED DESCRIPTION

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### [Detailed Description of the Invention]

#### [0001]

[Industrial Application] This invention relates to a multilayered circuit board by which two or more circuit patterns were formed via the insulating layer on the insulating substrate and which is used as a printed wired board, and a manufacturing method for the same.

#### [0002]

[Description of the Prior Art] In order to make density of wiring per circuit board high and to attain multi-functionalization or miniaturization in the circuit board in which the circuit pattern was formed on the insulating substrate, The multilayered circuit board which has an interstitial viahole, and the multilayered circuit board by which two or more circuit patterns were laminated via the insulating layer on the insulating substrate are developed variously, and is proposed.

[0003] As a typical multilayered circuit board known conventionally, there is the following, for example. The "double-sided circuit board" as used in the following explanation means the circuit board by which the circuit pattern of one layer each was provided in rear surface both sides of the substrate.

[0004](1) In ahefitters 33.2-33.8 of PRINTED CIRCUITS HANDBOOK (the 3rd edition; 1988 issue). As shown in drawing 2, it has the circuit pattern 104 to both sides, And via the prepreg 101 which the double-sided circuit board 105 and 105' which have the through hole 103 formed by plating a breakthrough become from adhesive resin. The multilayered circuit board which made connection between circuit patterns of the double-sided circuit board laminated by forming the through hole 102 which is laminated and penetrates total layers is indicated.

[0005](2) In 103-108 pages of an electronic industry material (the April, 1991 item). As shown in drawing 3, the 1st layer circuit pattern 108 is formed on the insulating substrate 106, The 2nd layer circuit pattern 109 and 3rd layer circuit pattern 109' which were formed from the metal skin via the insulating layer 107 and 107' on this circuit pattern are formed one by one, The multilayered circuit board which formed the through hole 102 which the 4th [ further ] layer or the circuit pattern beyond it is formed, and penetrates total layers, and connected the voltage plane 110 to the outermost layer is indicated.

[0006](3) In the Japanese publications of unexamined utility model applications 16482/1988. As shown in drawing 4, the circuit pattern 108 of the 1st layer which the metal skin formed on the insulating substrate 106 is formed, They are formed one by one by the circuit pattern 109 and 109' which were formed from the metal skin via the insulating layer 107 and 107' on the circuit pattern of this 1st layer, and to the insulating layer between circuit patterns. The interstitial viahole 111 with which it filled up so that conductive paste might serve as the same surface as an insulation layer is formed, and the circuit board which the electrical link between circuit patterns accomplished by this is proposed.

#### [0007]

[Problem(s) to be Solved by the Invention] Although the multilayered circuit board shown in (1) among the above is a popular thing put in practical use now, In this multilayer substrate, in order to laminate two or more double-sided circuit boards 105 and 105' which were manufactured separately via the prepreg 101, very high accuracy is required at the alignment between the circuit boards. That is, it is [ after laminating two or more circuit boards ] required for the through hole 102 in which total layers are penetrated and provided to have penetrated the predetermined part certainly in the circuit pattern of each class, and shortly after the position of this lamination is out of order, a defect occurs. Therefore, in each circuit pattern, the margin needed to be given to some extent, this penetrated part needed to be secured, and it had become the densification of wiring with the obstacle. When the through hole 102 which penetrates total layers performed the flow between this through hole and the circuit pattern located in an interlayer, the

touch area of both ends was small and there was a problem in the reliability of an electrical link. Since a through hole was established also in the circuit pattern which does not need a flow, the flexibility of wiring was restricted and the densification of wiring was checked by this.

[0008]In the manufacturing process of a unit circuit board, it the above-mentioned multilayered circuit board not only needs at least two plating, but needed the laminating process of a unit circuit board, the hole down after lamination, plating, etc., and it was very complicated on manufacture.

[0009]The multilayered circuit board shown in (2) also penetrated total layers, forms the through hole 102, and had become the advancement of wiring density with the obstacle. [ as well as the multilayered circuit board of the above (1) ] A circuit pattern is laminated by only one side of an insulating substrate, the grade of the increase in the number of the electric connection terminals between the circuit patterns accompanying the increase in the number of layers of a circuit pattern is large, and the densification of wiring was checked by this.

[0010]In manufacture of the above-mentioned multilayered circuit board, in order to carry out 1 stratification of the circuit pattern, formation and plating of the insulating layer needed to be performed once, respectively, and even after forming all the circuit patterns, hole down, plating, etc. were needed, and the room for an improvement was on manufacture.

[0011]The multilayered circuit board shown in (3) is connected by filling up with conductive paste the opening in which two or more circuit patterns laminated via the insulating layer were provided by this insulating layer. However, the conductive paste which this was filled up with this opening since the bottom of the hole was closed unlike the breakthrough, and was hardened can tend to do an opening, and the room of improvement is between the circuit pattern planes which contact by contraction at the time of hardening in the reliability of the electrical link of this portion. Like the above (2), only one side of an insulating substrate laminates, the grade of the increase in the number of the electric connection terminals between the circuit patterns over the increase in the number of layers of a circuit pattern was large, the densification of wiring was checked by this, and the circuit pattern was.

[0012]In manufacture of the above-mentioned multilayered circuit board, whenever it is required to harden independently the conductive paste with which the insulating layer and the opening were filled up for each class and it connects between circuit patterns once, it receives no less than 2 times of heat histories, and a manufacturing process is not only complicated, but the problem of degradation by the heat of the substrate itself arises.

[0013]In the multilayered circuit board of the above (2) and (3), since mounting of electronic parts was also restricted to one side, the fall of packaging density had also been caused.

[0014]Therefore, the purpose of this invention cancels the conventional problem mentioned above, and its reliability of the electrical link between each laminated circuit pattern is high, and there is in the densification of wiring being attained and providing a multilayered circuit board in which the densification of the packaging density of parts is possible, and a manufacturing method for the same.

[0015]

[Means for Solving the Problem]This invention persons repeated research wholeheartedly that the above-mentioned purpose should be attained. As a result, form a circuit pattern of the 1st layer in both sides of an insulating substrate, and. When the surface created by filling up with a conductive substance a breakthrough which penetrates this insulating substrate, and forming a through hole part uses a double-sided circuit board by which flattening was carried out, Form a metal skin in that it is very highly precise and formation of an insulating layer and formation of a circuit pattern from a metal skin can be performed on this double-sided circuit board, and both sides of this double-sided circuit board via an insulating layer, and by this metal skin. By performing an electrical link of between formation of a circuit pattern, and a circuit pattern or a circuit pattern, and a through hole part, Since a circuit pattern with high flexibility was formed without providing separately a through hole part penetrated to total layers, it found out that densification of wiring can be attained, and that electronic parts could be further mounted in both sides since a circuit pattern is laminated to both sides of a double-sided circuit board. In a manufacturing process, since a circuit pattern was laminated to both sides of a double-sided circuit board, processing for formation of an insulating layer, formation of a metal skin, and circuit pattern formation from this metal skin could be performed to double-sided coincidence, and it found out that increase in efficiency of a manufacturing process could be attained.

[0016]Namely, this invention has the 1st layer circuit pattern provided in both sides of an insulating substrate, . And fill up with a conductive substance a breakthrough which penetrates an insulating substrate, and have the through hole part formed so that the end face of this packing might turn into the surface of this 1st layer circuit pattern at the same flat surface mostly. It is a multilayered circuit board

including the 2nd layer circuit pattern that consists of a metal skin by which the surface was established in at least one surface of a flat double-sided circuit board and this double-sided circuit board via an insulating layer, An electrical link between this 2nd layer circuit pattern and this through hole part, An opening is formed in this insulating layer and a multilayered circuit board accomplished by covering an exposed part of a wall of this opening and the end face of said through hole part with a metal skin which continues a metal skin of the 2nd layer circuit pattern is provided so that at least a part of end face of this through hole part may be exposed.

[0017]This invention has the 1st layer circuit pattern provided in both sides of an insulating substrate as a manufacturing method of the above-mentioned multilayered circuit board, And fill up with a conductive substance a breakthrough which penetrates an insulating substrate, and the surface which has the through hole part formed so that the end face of this packing might turn into the surface of this 1st layer circuit pattern at the same flat surface mostly produces a flat double-sided circuit board, So that at least a part of end face of this through hole part may be exposed on at least one surface of this double-sided circuit board, An insulating layer in which an opening was formed is provided, an exposed part of a wall of an outside surface of this insulating layer and this opening and the end face of said through hole part is covered with a continuous metal skin, and a manufacturing method of a multilayered circuit board containing a method of etching a prescribed spot of this metal skin and forming the 2nd layer circuit pattern is also provided.

[0018]A sectional view of a multilayered circuit board of a typical mode of this invention is shown in drawing 1 and drawing 5.

[0019]As shown in the above-mentioned drawing, a multilayered circuit board of this invention, It has the 1st layer circuit pattern 2 and 2' which were formed in both sides of the insulating substrate 1, And the double-sided circuit board 5 with the flat surface which fills up with the conductive substance 4 the breakthrough 3 which penetrates this insulating substrate, and has the through hole part A processed and formed so that the end face of this packing might turn into mostly the surface of the 1st layer circuit pattern 2 and 2' at the same flat surface is included. The 2nd layer circuit pattern 7 and 7' which consist of metal skins via the insulating layer 6 are formed in rear surface both sides of the double-sided circuit board 5. The opening 8 is formed in the insulating layer 6 so that a part of end face of the through hole part A may be exposed, and another opening 8' is also provided in the insulating layer 6 so that a part of terminal area 9 of the 1st layer circuit pattern 2 may be exposed. A metal skin which continued over an exposed surface of lateral surface of the insulating layer 6, the opening 8 and a wall of 8', and a through hole part and an exposed surface of the terminal area 9 is covered, and the 2nd layer circuit pattern 7 and 7' are formed by etching a necessary place of a metal skin on the insulating layer 6. An electrical link between the 2nd circuit pattern 7, and 7' and the through hole part A and an electrical link between the 1st layer circuit pattern and the 2nd layer circuit pattern are attained by metal skin which continued [ above-mentioned ].

[0020]What has publicly known construction material and structure as the above-mentioned insulating substrate 1 is used without restriction. If a typical thing is illustrated, a paper base-phenol resin laminated circuit board, a paper base-epoxy resin laminated circuit board, A paper base-polyester resin laminated circuit board, a glass base material-epoxy resin laminated circuit board, A paper base-Teflon-resin laminated circuit board, a glass base material-polyimide resin laminated circuit board, A glass base material-BT (bismaleimide triazine) resin resin laminated circuit board, A metal system insulating substrate which covered and carried out the insulation process of the metal plates, such as flexible substrates, such as synthetic resin bases, such as a composite resin substrate, polyimide resin, polyester resin, aluminum which provided a breakthrough, iron, stainless steel, with an epoxy resin etc., or a ceramics board is mentioned.

[0021]Publicly known construction material which has conductivity can use especially the circuit pattern 2 of the 1st layer formed in both sides of the insulating substrate 1, and construction material of 2' without restriction. If typical construction material is illustrated, copper, nickel, aluminum, etc. will be mentioned. Before long, copper is used most suitably. Although not restricted in particular about thickness of the above-mentioned circuit pattern, either, generally 5-70 micrometers is suitable.

[0022]In the above-mentioned double-sided circuit board, it is [ packing / 4 / which has conductivity in the breakthrough 3 provided in a predetermined part of an insulating substrate by penetrating an insulating substrate ] smooth in the end face, and it is filled up and the through hole part A is formed so that the same flat surface may be mostly made with both the surfaces of a double-sided circuit board. Packing which has this conductivity is used that publicly known construction material does not especially have restriction. For example, a cured body of hardenability conductive material which gives a cured body which

has conductivity is typical. As this hardenability conductive material, publicly known hardenability conductive material which mixed electrical conducting materials, such as gold, silver, copper, nickel, lead, and carbon, and thermosetting resin of publicly known cross-linking, such as an epoxy resin and phenol resin, with an organic solvent as occasion demands, and was made into paste state can be used.

[0023]As for the above-mentioned hardenability conductive material, in order to form a through hole part which has good conductivity, it is preferred that electrical resistance after hardening adjusts [ below  $1 \times 10^{-2}$  omega-cm ] selection of an electrical conducting material and the amount of each ingredient used as.

[0024]A path in particular of a through hole part is not restricted, and can be set up arbitrarily. What is necessary is just more than an aperture which is a grade which can generally be filled up with said hardenability conductive material, and, specifically, it is the range of 0.3-2 mm preferably 0.2 mm or more.

[0025]In formation of the above-mentioned through hole part, if the outermost layer of packing which has the conductivity with which the breakthrough 3 is filled up is formed by a metal skin, the electric reliability of a through hole part can be improved further.

[0026]It is preferred for the 1st layer circuit pattern 2 of the above-mentioned double-sided circuit board, and an electrical link of 2' and the through hole part A to carry out by forming the land 11 in the circumference of this through hole part A in this 1st layer circuit pattern. In this case, in order to raise an electrical link of a land and a through hole part more, it is preferred to cover the end face of a land and a through hole part with the continuous metal skin 12. This metal skin 12 may be independently formed, as shown in drawing 1, and a metal skin for constituting the circuit pattern 7 and 7' which were laminated as shown in drawing 5 may be used.

[0027]In this invention, circuit Batang 7 and 7' of one or more layers which consist of a metal skin formed via the insulating layer 6 are formed in at least one surface of the above-mentioned double-sided circuit board 5.

[0028]What consists of publicly known construction material as the above-mentioned insulating layer 6 is especially used without restriction. For example, the publicly known hardenability insulating resin 52 (trade name: made by Ciba-Geigy) known as photosensitive insulation resist, for example, pro PIMA, the PUROPI coat 5000 (trade name: made by Nippon Paint Co., Ltd.), etc. are preferred. The thickness of an insulating layer should just be a grade which can maintain insulation between circuit patterns which exist in the both sides, and, generally a thickness of 20-100 micrometers is suitable for it.

[0029]As for the above-mentioned insulating layer surface, it is preferred to perform a surface roughening process in order to raise the adhesion of a metal skin formed in the surface. When a method of a surface roughening process immerses in a method, an alkaline potassium permanganate solution, and a chromic acid solution which are physically ground with a buff, a brush, etc., a method that a method of carrying out surface roughening chemically, etc. are publicly known is especially adopted without restriction.

[0030]Construction material also with a publicly known metal skin which constitutes a circuit pattern is especially used without restriction. For example, copper, nickel, etc. are mentioned. Before long, copper is used most suitably. thickness of a grade in which the thickness of the above-mentioned metal skin can demonstrate conductivity should just be secured -- usually -- a thickness of 50 micrometers or less -- a thickness of 5 micrometers -- about 35 micrometers is preferably preferred.

[0031]In this invention, the opening 8 for connecting between formed circuit patterns or a circuit pattern, and a through hole part exists in the insulating layer 6. This opening is provided so that a terminal area of a circuit pattern or at least a part of end face of a through hole part may be exposed. When connecting a circuit pattern comrade, the opening 8 is formed so that a terminal area of a circuit pattern of a side near a double-sided circuit board may be exposed. A grade by which an electrical link is attained by covering of the metal skin 10 described later may be sufficient as this exposure area. What is necessary is generally, just to expose area of a portion exposed from an insulating layer in area more than the nominal diameter phi of 50 micrometers. Shape in particular of an opening is not limited but should just adopt suitably shape of having been suitable for a design of a circuit pattern, such as circular, an ellipse form, a rectangle, and a square, again.

[0032]When a metal skin is not formed in these surfaces although the land 11 of the 1st layer circuit pattern is formed in the circumference of this through hole part A as shown in drawing 5, it is desirable to expose a metal surface of the end face of a through hole part, and to make it expose to area which contains this land further. And a land and a through hole part of a wall of this opening and the 1st layer circuit pattern exposed by this opening are covered with a metal skin of a laminated circuit pattern, and a continuous metal skin. For example, in drawing 5, a metal skin which constitutes circuit pattern 7', and structure covered with continuous metal skin 12' are shown in the land 11 of 1st layer circuit pattern 2'

and the end face of the through hole part A which were exposed by the opening 8.

[0033]An electrical link of 1st layer circuit pattern 2' and the end face of the through hole part A, It is also possible to carry out by a mode covered with a metal skin which forms an opening in an insulating layer, for example so that a part of end face of a through hole part and a terminal area of the 1st layer circuit pattern may be exposed, and continues this exposed part and an insulating layer in the meantime in addition to the above-mentioned circuit mode.

[0034]Structure of a multilayer substrate publicly known as other structures of a multilayered circuit board of this invention is especially adopted without restriction. For example, although not shown in a figure, it is preferred to provide a good layer of tolerance by a solder resist in a part of a required request of the outermost layer.

[0035]Although a multilayered circuit board of a mode shown in drawing 1 and drawing 5 showed an example of the four-layer circuit board which formed a circuit pattern of one layer via an insulating layer, respectively on the 1st layer circuit pattern that exists in both sides of a double-sided circuit board, Structure which is not limited to this and laminated the circuit board further via an insulating layer on this circuit pattern is also possible for this invention. Such an example is shown in drawing 11 (1) – (4).

[0036]That is, drawing 11 shows 2nd layer circuit pattern 7, the 3rd layer circuit pattern 19 that becomes the surface of 7 from a metal skin via the insulating layer 18, and an embodiment of shoes for 19' to be formed in. (1) of drawing 11 is a mode in which the 3rd layer circuit pattern was formed on the 2nd [ of a multilayered circuit board of a mode shown in drawing 5 ] circuit pattern. (2) of drawing 11 is a mode in which the 3rd layer circuit pattern was formed on the 2nd [ of a multilayered circuit board of a mode shown in drawing 1 ] circuit pattern. A mode shown in (3) and (4) shows a mode to which the 2nd layer circuit pattern connected with this through hole part one by one and the 3rd layer circuit pattern exist in a position of a through hole part, or a mode which carried out direct continuation of the 3rd layer circuit pattern to a through hole part via the 2nd layer circuit pattern.

[0037]In these modes, an electrical link with formation and other layers of the insulating layer 18 and the 3rd layer circuit pattern, or a through hole part is performed according to a formation method of said insulating layer 6 and the 2nd layer circuit pattern.

[0038]For example, a metal skin is formed and formation of the 3rd layer circuit pattern is performed by etching a predetermined part, after forming an insulating layer which forms an opening in a predetermined part. The 3rd layer circuit pattern, other circuit patterns, and an electrical link with a through hole part, The opening 21 is formed in the insulating layer 18 so that the terminal area 9 of the 1st layer circuit pattern, the terminal area 20 of the 2nd layer circuit pattern, or at least a part of end face of the through hole part A may be exposed, The 3rd layer circuit pattern, the 2nd layer circuit pattern, the 1st layer circuit pattern, or a through hole part is connectable by covering the side and this exposed part of this opening with the 3rd layer circuit pattern 19, a metal skin which forms 19', and a continuous metal skin.

[0039]What is necessary is to provide an opening in the insulating layer 6 and the insulating layer 18 one by one, as shown in (4), and just to perform covering by said metal skin in the above-mentioned connection, when carrying out direct continuation of the 3rd layer circuit pattern, the 1st layer circuit pattern, or the through hole part.

[0040]The following methods will be mentioned if a typical manufacturing method of a multilayered circuit board of this invention is illustrated.

[0041]That is, drawing 6 shows a process of manufacturing a multilayered circuit board, with a sectional view. As shown in this figure, it has the 1st layer circuit pattern 2 and 2' to both sides of the (1) insulating substrate 1, The surface which was filled up with the packing 4 which has the breakthrough 3 which penetrates this insulating substrate, and has conductivity in this breakthrough and in which the through hole part A was formed on and at least flat one surface of the double-sided circuit board 5. (2) After covering with the insulating layer 6 so that the opening 8 to which the terminal area 13 of the 2nd layer circuit pattern formed on the 1st above-mentioned layer circuit pattern and the 1st layer circuit pattern to be connected and the through hole part A are exposed may be formed, (6) Form the metal skin 10 for a flow which follows the circuit pattern 7 of the 2nd more than layer, 7', and this circuit pattern by covering a wall and an insulating layer surface of this exposed part and the opening 8 with the metal skin 14, etching a prescribed spot of (4) this metal skin, and forming a circuit pattern.

[0042]A formation method in particular of the above-mentioned insulating layer 6 is not limited, but a publicly known method is adopted without restriction. Generally, hardenability insulating resin hardened with a various light or heat of a gestalt, such as a dry film, liquid resist, a dry film, and fluid resist concomitant use, can be used. What is necessary is to use the above-mentioned hardenability insulating resin, to choose methods, such as print processes and a photographic method, suitably according to fine degree,

and just to adopt them as a formation method of this insulating layer. For example, an insulating layer can be formed by laminating hardenability insulating resin layers hardened by the exposure of light, such as liquid resist and a dry film, all over a double-sided circuit board, and removing an uncured part by development after irradiating with light except for a part to be formed [ of an opening ].

[0043]Since thickness accuracy of an insulating resin layer is also good and can also be formed in a table and rear-face coincidence by an above-mentioned method if a dry film hardened by light is used for formation of an insulating layer, it is more efficiently highly precise and an insulating layer can be formed.

[0044]As for a size of the opening 8 of the above-mentioned insulating layer 6, in a mode shown in drawing 6, it is preferred to consider it as a size of said range from which an electrical link is obtained by a metal skin.

[0045]Drawing 7 shows a mode which uses a double-sided circuit board which does not form the metal skin 12 to a mode shown in drawing 6. In this case, in order to ensure a flow with the required through hole part A of 1st layer circuit pattern 2' and an electrical link, the opening 8 provided in the insulating layer 6 is formed so that a whole surface product of the end face of this through hole part A and the land 11 of a circuit pattern of that circumference may be exposed. By doing in this way, an exposed portion is simultaneously plated by formation of the continuing metal skin 14, and an electrical link of this portion can be performed certainly.

[0046]According to the process shown in above-mentioned drawing 7, it is also more possible than a process shown in drawing 6 to reduce a plating process as 1 \*\*.

[0047]In said method, although how in particular to form the metal skin 14 is not restricted, generally a metaled electroless deposition method is preferred.

[0048]In order to form a circuit pattern from a metal skin, the same method as formation of said 1st layer circuit pattern is applicable. Generally an etching method is preferred.

[0049]In this invention, it is still more possible to laminate an insulating layer and a circuit pattern one by one similarly on a circuit pattern of the 2nd layer.

[0050]Especially the above-mentioned circuit pattern laminated is used without being restricted to a signal wire, a power source wire, a ground wire, and an electromagnetic wave shield layer.

[0051]Although the end face of the through hole part A of a double-sided circuit board showed a mode beforehand covered with the metal skin 12 by drawing 6, this metal skin is not indispensable.

[0052]When not forming this metal skin, as shown in drawing 7, a metal skin may be provided and formed at the time of formation of the 2nd layer circuit pattern so that a metal skin of this circuit pattern may be followed. Namely, this insulating layer is formed so that the land 11 of the 1st layer circuit pattern formed in the end face of the through hole part A which needs to be connected with the 1st layer circuit pattern, and its circumference in drawing 7 may be exposed by an opening of the insulating layer 6, A mode which plates this exposed portion simultaneously at the time of formation of the continuing metal skin 14 is shown.

[0053]A concrete manufacturing method in particular of a double-sided circuit board is not restricted, and what is necessary is just to determine it suitably in the above-mentioned manufacturing method according to structure of a multilayered circuit board obtained. If a manufacturing method of this double-sided circuit board is illustrated, a double-sided circuit board which a method of showing a double-sided circuit board used for a manufacturing process shown, for example in said drawing 6 in drawing 8 uses for a manufacturing process shown in said drawing 7 again will be mentioned as a method with a typical method shown in drawing 9.

[0054]Namely, in drawing 8, the breakthrough 3 for through holes is formed in the insulating substrate 1 which has the conductive layer 15 to both sides, It is filled up and hardenability conductive material which gives the cured body 4 which has conductivity to this breakthrough is stiffened so that this cured body may project from a breakthrough after hardening, After grinding smoothly and forming the through hole part A in said conductive layer side so that the surface constituted by this conductive layer and cured body may turn into the same flat surface mostly, The metal skin 16 is formed in the smoothed this surface, and a mode which obtains a double-sided circuit board is shown by by etching a prescribed spot of a conductor layer which consists of this conductive layer and a metal skin, and forming the 1st layer circuit pattern 2 and 2'. In drawing 9, the breakthrough 3 for through holes is formed in the insulating substrate 1 which has the conductive layer 15 to both sides, It is filled up and hardenability conductive material which gives the cured body 4 which has conductivity to this breakthrough is stiffened so that this cured body may project from a breakthrough after hardening, After grinding smoothly and forming the through hole part A between said conductive layers so that a field constituted by this conductive layer and cured body may turn into the same flat surface mostly, a mode which obtains a double-sided circuit board is shown by by etching a

prescribed spot of the above-mentioned conductive layer, and forming the 1st layer circuit pattern 2 and 2'.

[0055]Hereafter, the above-mentioned process is explained still in detail.

[0056]A raw material substrate which provided a conductive layer in both sides of the insulating substrate 1 is used that publicly known things, such as what pasted together metallic foils, such as what formed metal layers, such as copper, by plating on an insulating substrate, and copper, by adhesion, do not especially have restriction.

[0057]The breakthrough 3 for through hole part formation is first formed in an insulating substrate which has a conductive layer to both sides. The path of the above-mentioned breakthrough should just choose a path corresponding to a path of a through hole part made into the purpose. It is used without limiting the publicly known means in particular same as a formation method of the above-mentioned breakthrough 3 as manufacture of the usual circuit boards, such as drilling processing, punching work, and laser processing. In this case, in order to raise the reliability of an electrical link of a cured body of hardenability conductive material and a conductive layer with which the breakthrough 3 is filled up, an inclined plane may be made to exist in a conductive layer located in a periphery of this breakthrough, and a touch area with this cured body may be increased. A method of a periphery of a conductive layer in the above-mentioned breakthrough in which an inclined plane is made to exist in part at least, a method of performing soft etching with soft etching liquid, and forming this inclined plane, after forming a breakthrough for through holes in an insulating substrate which has a conductive layer to both sides -- or, After forming a breakthrough, it can use without limiting a method in particular of forming around a breakthrough, and etching and forming etching resist which has a big path for a while with a little big drill of a path, rather than a method of grinding a conductive layer and an insulating layer on a taper, and a breakthrough, etc. rather than a breakthrough.

[0058]As for packing which has the conductivity which exists in the through hole part A of a double-sided circuit board, it is preferred to form the above-mentioned hardenability conductive material in the breakthrough 3 of an insulating substrate by filling up and hardening.

[0059]As for restoration to a breakthrough of hardenability conductive material, a method with which it is filled up to such an extent that this hardenability conductive material fills the whole space of a breakthrough and it specifically projects 0.1-2 mm preferably 0.05 mm or more a little from both the surfaces of a conductive layer is recommended. A method of performing spreading of 1 time or multiple times by print processes if a typical method of being filled up with this hardenability conductive material is illustrated. It is filled up by a method, a roll coater, or a curtain coating machine pressed fit by a squeegee of a rear surface couple from the rear surface both-sides side of an insulating substrate, and means, such as the method of scratching an excessive paint by a squeegee, are used suitably.

[0060]What is necessary is for hardening of hardenability conductive material with which a breakthrough was filled up to choose suitably a thing suitable for hardening of hardenability conductive material, and just to stiffen it from publicly known curing methods, such as a hot blast stove, an infrared furnace, a far-infrared furnace, an ultraviolet curing furnace, and electron beam curing oven.

[0061]It is important to grind both the surfaces smoothly so that the surface of a conductive layer and the surface constituted by cured body of hardenability conductive material may turn into the same surface mostly after hardening hardenability conductive material. That is, in formation of a circuit pattern which is a post process, formation of a pattern by etching resist and etching can be performed with sufficient accuracy, and this polish enables it to also form an insulating layer to this circuit pattern top with sufficient reliability further.

[0062]Generally a method used for polish usual [ , such as slurry polish, buffing, and scrub polish, ] as a method of grinding smoothly the surface constituted with a conductive layer and hardenability conductive material as mentioned above is used.

[0063]In drawing 8, a mode which forms the metal skin 16 on a field where the conductive layer 15 containing the through hole part A was smoothed is shown. Before forming the 1st layer circuit pattern by leaving a conductive layer so that this metal skin may be formed and the land 11 may be formed on these outskirts of a through hole part by continuing etching, a through hole part and a land of a circuit pattern can be covered with a common metal skin. Electric reliability by a through hole part improves by formation of this metal skin. Of course, it is also possible to carry out, when laminating the 2nd layer circuit pattern via an insulating layer, as covering with a through hole part by the above-mentioned metal skin and a land of a circuit pattern was explained about drawing 7.

[0064]A formation method of the above-mentioned metal skin 16 can be performed with a chemical-plating method or an electroplating method. Although construction material of this metal skin is used without

restricting a publicly known conductive metal in particular, it is preferred to choose the same construction material as conductive metals, such as copper used as construction material of hardenability conductive material which generally gives a cured body which has said conductivity. Although restriction in particular is not carried out, thickness of a metal skin is usually 50 micrometers or less in thickness, and is good to carry out at 5 micrometers – about 35 micrometers preferably.

[0065]As mentioned above, as shown in a process of (5) to (7) of drawing 8 and drawing 9, the 1st layer circuit pattern is formed in a smoothed field of a through hole portion, a conductive layer or a conductive layer, and a metal skin.

[0066]That is, a formation method of the 1st layer circuit pattern has a common method of etching by forming an etching pattern by the etching resist 17. Especially, etching resist used here is used without restriction, and a dry film, resist ink, etc. should just use it by fine degree of a pattern, choosing it suitably. The etching resist pattern should just adopt a positive pattern or a negative pattern suitably with an etching method. For example, what is necessary is just to adopt a negative pattern in an etching method represented with an etching method represented by tenting by the solder exfoliating method and the SES method in a positive pattern.

[0067]

[Effect of the Invention]According to this invention, form the circuit pattern of the 1st layer in both sides of an insulating substrate so that I may be understood from the above explanation, and. . Filled up with the conductive substance the breakthrough which penetrates this insulating substrate, formed the through hole part and were constituted. When the surface forms the 2nd layer circuit pattern by formation and the metal skin of an insulating layer on this double-sided circuit board using the double-sided circuit board by which flattening was carried out, it is very highly precise and formation of the 2nd layer circuit pattern this laminated can be performed. By formation of the metal skin which continues at formation and it of an insulating layer at both sides of this double-sided circuit board. Since a circuit pattern can be formed with high flexibility, without providing separately the through hole part penetrated to total layers by performing between formation of a circuit pattern, and a circuit pattern or a circuit pattern, and the electrical link of a through hole part, it is possible to attain densification of wiring.

[0068]In a manufacturing process, since a circuit pattern can be laminated to both sides of a double-sided circuit board, processing for formation of an insulating layer, formation of a metal skin, and the circuit pattern formation from this metal skin can be performed to double-sided coincidence, and the increase in efficiency of a manufacturing process can be attained.

[0069]Since the circuit pattern is formed in both sides, electronic parts can be mounted in both sides again.

[0070]

[Example]Hereafter, in order to explain this invention concretely, an example is shown, but this invention is not limited to these examples.

[0071]The double-sided circuit board was manufactured according to the process shown in example 1 drawing 8, and the multilayered circuit board was manufactured according to the process shown in drawing 6 using this double-sided circuit board.

[0072]That is, as shown in drawing 8, the 1.6-mm-thick glass base material epoxy resin copper-clad laminate sheet was used for (1) both sides as the insulating substrate 1 which has the conductive layer 15, and the breakthrough 3 with a (2) diameters of 0.4 mm was formed by drilling. (3) As the hardenability conductive material 4, this breakthrough 3 was filled up with commercial thermosetting silver paste (the product made by \*\*\*\*\*PS-652 (trade name)) with screen printing so that the cured body might project a little from the breakthrough 3. The packing 4 which carries out at 80 \*\* with a hot air drying furnace, carries out dry hardening of this silver paste on the conditions of 2 hours at 150 \*\* for 4 hours, and has conductivity was constituted. (4) The field which used the buff of No. 320 and No. 600 one by one next, and the cured body of the hardened silver paste projected was ground, and the conductive layer surface containing this cured body was smoothed. Subsequently, electroplating was performed to the smoothed conductive layer surface containing the through hole (4') part A. The plating bath used Nihon Schering KAPARASHIDO GS (trade name), and formed the 10-micrometer-thick copper plating layer 16 on condition of current density 2 A/dm<sup>2</sup>.

[0073]Subsequently, the dry film (1.5 mil of "Aqua Maher CF" by Hercules) was laminated and developed [ exposed and ] on the conductive layer surface by which (5) smoothing was carried out as the etching resist 17, and the resist pattern was formed in it. Then, the 1st layer circuit pattern 2 which has the land 11, and the double-sided circuit board 5 which has 2' were obtained by etching with (6) cupric-chloride

etching reagent, and exfoliating (7) etching resist.

[0074] Subsequently, as shown in drawing 6, in order to form an insulating layer on the 1st layer circuit pattern which contains (2) through hole parts A using the (1) above-mentioned double-sided circuit board 5, Photosensitive insulation resist (PUROPI coat 5000: a trade name, the Nippon Paint Co., Ltd. make) was applied, and it dried, and post heating hardening was carried out and the pattern which has the opening 8 of the insulating layer 6 into the portion which performed exposure and development, and which needs an electrical link was formed. Next, after carrying out a surface roughening process for the (3) above-mentioned insulating layer surface, electroless deposition and electrolytic plating were performed to the both sides, and the 10-micrometer-thick copper plating layer 14 was formed in them. Subsequently, the etching resist 17 used for the (4) copper-plating-layer 14 surface above (5) is laminated, After having exposed and developed negatives, forming the resist pattern and etching with a ferric chloride etching reagent, the circuit pattern 7 and the multilayered circuit board which forms 7' and has a circuit pattern of four layers were obtained by exfoliating etching resist.

[0075] It was 31mohm as a result of measuring resistance between the circuit pattern 7 linked to the through hole which locates and is common in the rear surface of the obtained multilayered circuit board, and 7'. the spalling test (-65 \*\*x 30 minutes <- ->125 \*\*x 30 minutes) (in drawing 10 -- (1)- (1.) of JIS C-5012 which uses this circuit pattern 7 located in the rear surface of a multilayered circuit board as shown in drawing 10, and a test pattern including between 7' In the measure resistance between (2)-(2) and (3)-(3), even if it passed over 500 times in the number of cycles, there is a flow of this circuit pattern 7 located in the rear surface of the above-mentioned multilayered circuit board and a test pattern including between 7', and there was also almost no rise of subsequent electric resistance.

[0076] The double-sided circuit board was manufactured according to the process shown in example 2 drawing 9, and the multilayered circuit board was manufactured according to the process shown in drawing 7 using this double-sided circuit board.

[0077] That is, as shown in drawing 9, the 1.6-mm-thick glass base material epoxy resin copper-clad laminate sheet was used for (1) both sides as the insulating substrate 1 which has the conductive layer 15, and the breakthrough 3 with a (2) diameters of 0.4 mm was formed by drilling. (3) As the hardenability conductive material 4, this breakthrough 3 was filled up with commercial thermosetting silver paste (the product made by \*\*\*\*\*PS-652 (trade name)) with screen printing so that the cured body might project a little from the breakthrough 3. The packing 4 which carries out at 80 \*\* with a hot air drying furnace, carries out dry hardening of this silver paste on the conditions of 2 hours at 150 \*\* for 4 hours, and has conductivity was constituted. (4) The field which used the buff of No. 320 and No. 600 one by one next, and the cured body of the hardened silver paste projected was ground, and the conductive layer surface containing this cured body was smoothed.

[0078] Subsequently, the dry film (1.5 mil of "Aqua Maher CF" by Hercules) was laminated and developed [ exposed and ] on the conductive layer surface by which (5) smoothing was carried out as the etching resist 17, and the resist pattern was formed in it. Then, the 1st layer circuit pattern 2 which has the land 11, and the double-sided circuit board 5 which has 2' were obtained by etching with (6) ferric-chloride etching reagent, and exfoliating (7) etching resist.

[0079] Subsequently, as shown in drawing 7, in order to form an insulating layer on the 1st layer circuit pattern which contains (2) through hole parts A using the (1) above-mentioned double-sided circuit board 5, Photosensitive insulation resist (PUROPI coat 5000: a trade name, the Nippon Paint Co., Ltd. make) was applied, and it dried, and post heating hardening was carried out and the pattern which has the opening 8 of the insulating layer 6 into the portion which performed exposure and development, and which needs an electrical link was formed. In the portion which 1st layer circuit pattern 2' connects with a through hole part, this example shows the mode which formed the insulating layer 6 so that the through hole part A and the land 11 of the circumference might be exposed (in drawing 7, it is a lower part of the left-hand side through hole A).

[0080] Next, after carrying out the surface roughening process of the surface of the (3) above-mentioned insulating layer, electroless deposition and electrolytic plating were performed to the both sides, and the 10-micrometer-thick copper plating layer 14 was formed in them. Subsequently, the etching resist 17 used for the (4) copper-plating-layer 14 surface above (5) is laminated, After having exposed and developed negatives, forming the resist pattern and etching with a cupric chloride etching reagent, the circuit pattern 7 and the multilayered circuit board which forms 7' and has a circuit pattern of four layers were obtained by exfoliating etching resist.

[0081] It was 33mohm as a result of measuring resistance between the circuit pattern 7 linked to the through hole which locates and is common in the rear surface about the obtained multilayered circuit

board, and 7'. In the spalling test ( $-65^{\circ}\text{C} \times 30\text{ minutes} \leftarrow \rightarrow 125^{\circ}\text{C} \times 30\text{ minutes}$ ) of JIS C-5012 which uses this circuit pattern 7 located in the rear surface of a multilayered circuit board as shown in drawing 10, and a test pattern including between 7', Even if passed the number 500 times of cycles, there is a flow of the above-mentioned circuit pattern 7 and a test pattern including between 7', and it did not almost have the rise of subsequent electric resistance, either.

[0082]By a three or less-example method, the hardenability conductive material which consists of copper paste was prepared. Namely, mean particle diameter of 6.8 micrometers, tap density  $2.99\text{ g/cm}^3$ , Linolic acid was blended with the arborescence electrolytic copper powder of specific surface area  $2[\text{cm}^2/\text{g}]$  of 4200  $\text{cm}^2/\text{g}$  at a rate of  $0.25 \times 10^{-5}\text{ mmol/cm}^2$  to the copper powder surface, and preliminary mixing was carried out with the mortar for 15 minutes under a nitrogen atmosphere. Thus, to binder 100 weight section of neopentyl glycol glycidyl ether (weight per epoxy equivalent =150) / novolac-type-phenol-resin (hydroxy equivalent =105) =74 / 26 (weight ratio), carry out 456 weight-section addition and the obtained pretreatment copper powder further, After carrying out 2.8 weight-section addition to binder 100 weight section, 2-ethyl-4-methylimidazole was kneaded for 30 minutes by 3 roll mills, and was made into paste state.

[0083]In the method of Example 1, the multilayered circuit board was similarly manufactured except having used the above-mentioned copper paste for silver paste, having replaced it with.

[0084]It was 39mohm as a result of measuring resistance between the circuit pattern 7 linked to the through hole which locates and is common in the rear surface of the obtained multilayered circuit board, and 7'. In the spalling test ( $-65^{\circ}\text{C} \times 30\text{ minutes} \leftarrow \rightarrow 125^{\circ}\text{C} \times 30\text{ minutes}$ ) of JIS C-5012 which uses this circuit pattern 7 located in the rear surface of a multilayered circuit board as shown in drawing 10, and a test pattern including between 7', Even if it passed over 500 times in the number of cycles, there is a flow of the above-mentioned circuit pattern 7 and a test pattern including between 7', and it did not almost have the rise of subsequent electric resistance, either.

[0085]In example 4 Example 1, the circuit board was similarly manufactured except not having formed the copper plating layer 16 shown in (4') of drawing 8 in the smoothed conductive layer surface containing a through hole part.

[0086]It was 37mohm as a result of measuring resistance between the circuit pattern 7 linked to the through hole which locates and is common in the rear surface of the obtained multilayered circuit board, and 7'. In the spalling test ( $-65^{\circ}\text{C} \times 30\text{ minutes} \leftarrow \rightarrow 125^{\circ}\text{C} \times 30\text{ minutes}$ ) of JIS C-5012 which uses this circuit pattern 7 located in the rear surface of a multilayered circuit board as shown in drawing 10, and a test pattern including between 7', Although there was a flow of the circuit pattern 7 located in the rear surface of the above-mentioned multilayered circuit board to the 300 numbers of cycles and a test pattern including between 7', a rise of some of electric resistance began to be seen after that.

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[Translation done.]

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3. In the drawings, any words are not translated.

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## DESCRIPTION OF DRAWINGS

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### [Brief Description of the Drawings]

[Drawing 1]It is a sectional view showing one example of the multilayered circuit board of this invention.

[Drawing 2]It is a sectional view showing one conventional example of a multilayered circuit board.

[Drawing 3]It is a sectional view showing one conventional example now [ of a multilayered circuit board ].

[Drawing 4]It is a sectional view of a multilayered circuit board showing one conventional example now further.

[Drawing 5]It is a sectional view showing one example now [ of the multilayered circuit board of this invention ].

[Drawing 6]They are a series of sectional views showing one example of the manufacturing process of the multilayered circuit board of this invention.

[Drawing 7]They are a series of sectional views showing one example now [ of the manufacturing process of the multilayered circuit board of this invention ].

[Drawing 8]They are a series of sectional views showing the manufacturing process of the double-sided circuit board used for the manufacturing process of drawing 6.

[Drawing 9]They are a series of sectional views showing the manufacturing process of the double-sided circuit board used for the manufacturing process of drawing 7.

[Drawing 10]It is a figure showing the pattern for spalling tests according to JIS C-5012 to the multilayered circuit board of this invention.

[Drawing 11]It is a sectional view which illustrates the multilayered circuit board of this invention which has a circuit pattern of three layers on one side.

### [Description of Notations]

1 Insulating substrate

2 The 1st layer circuit pattern

The 2' 1st layer circuit pattern

4 Conductive substance

5 Double-sided circuit board

6 Insulating layer

7 The 2nd layer circuit pattern

The 7' 2nd layer circuit pattern

8 Opening

8' opening

9 The terminal area of a pattern

10 Metal skin

11 Land

12 Metal skin

12' metal skin

13 Terminal area

14 Metal skin

15 Conductive layer

16 Metal skin

17 Etching resist

101 Prepreg

102 Common through hole

103 Through hole

104 Circuit pattern  
105 Double-sided circuit board  
105' double-sided circuit board  
106 Insulating substrate  
107 Insulating layer  
108 The 1st layer circuit pattern  
109 The 2nd layer circuit pattern  
The 109' 3rd layer circuit pattern

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[Translation done.]

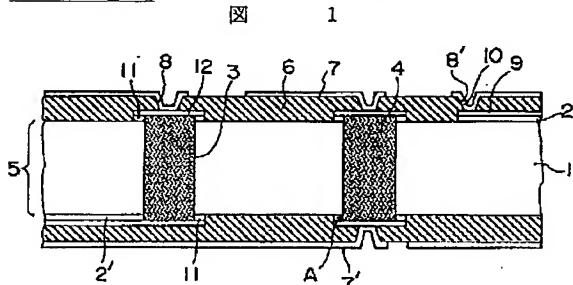
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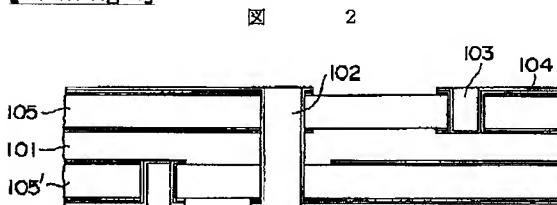
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## DRAWINGS

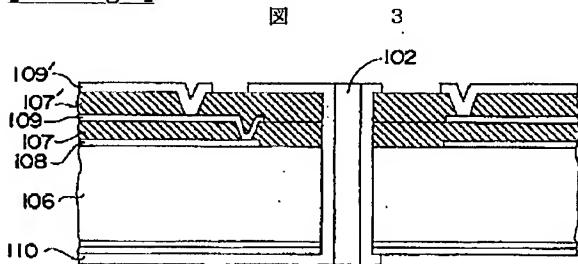
## [Drawing 1]



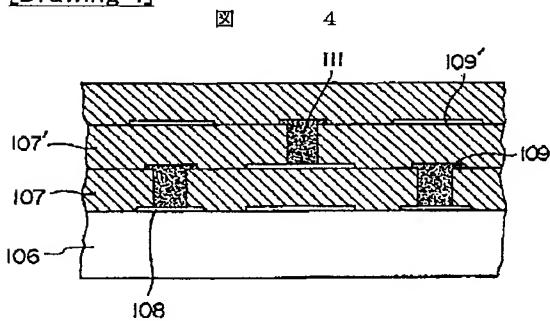
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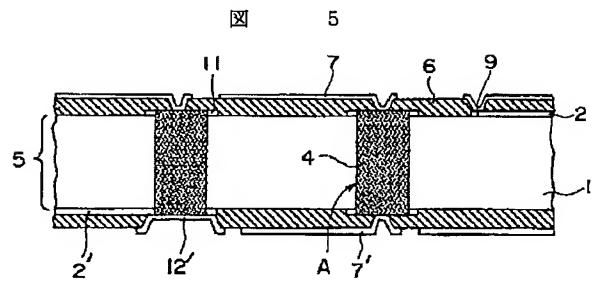
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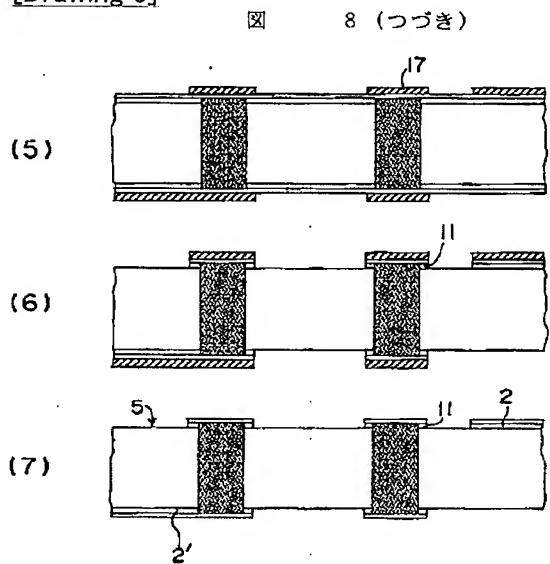
## [Drawing 4]



## [Drawing 5]

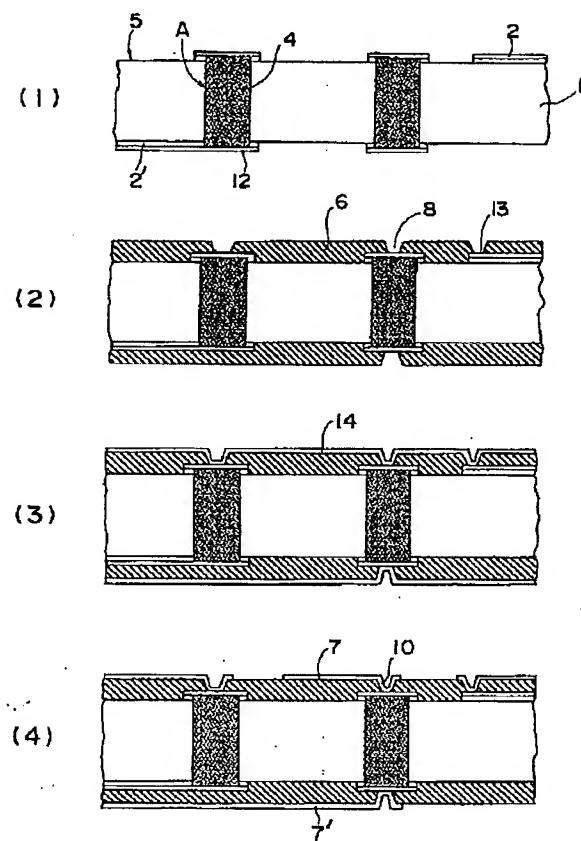


[Drawing 9]



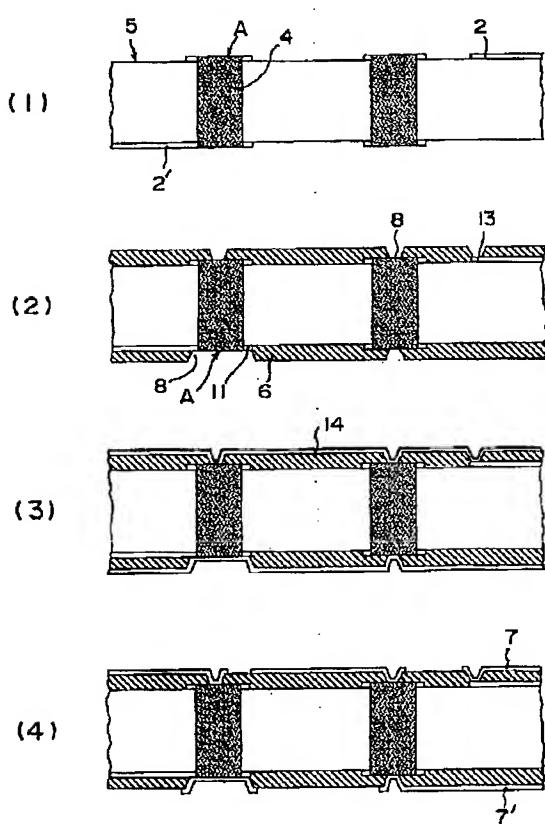
[Drawing 6]

図 6



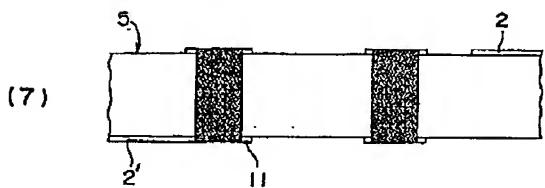
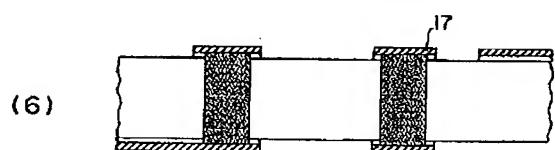
[Drawing 7]

図 7



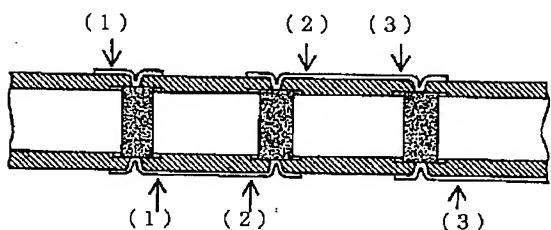
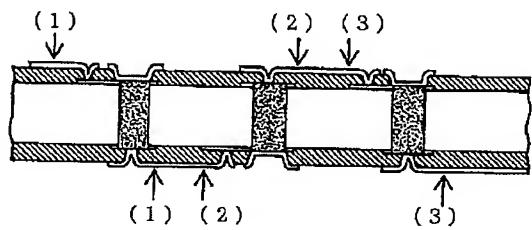
## [Drawing 11]

図 9 (つづき)



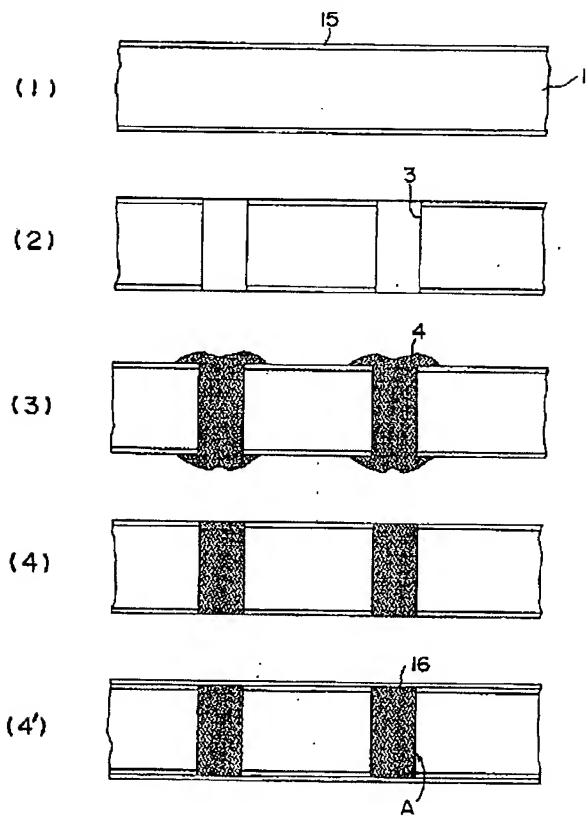
## [Drawing 12]

図 10



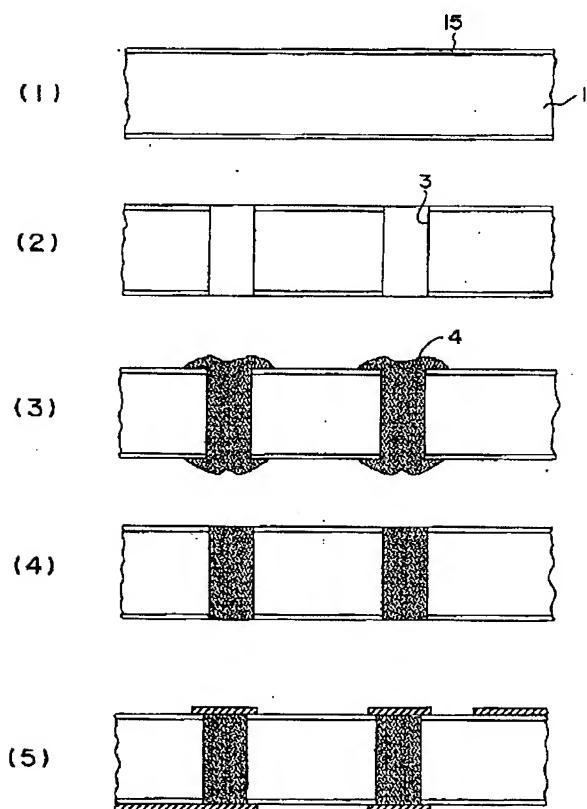
## [Drawing 8]

図 8



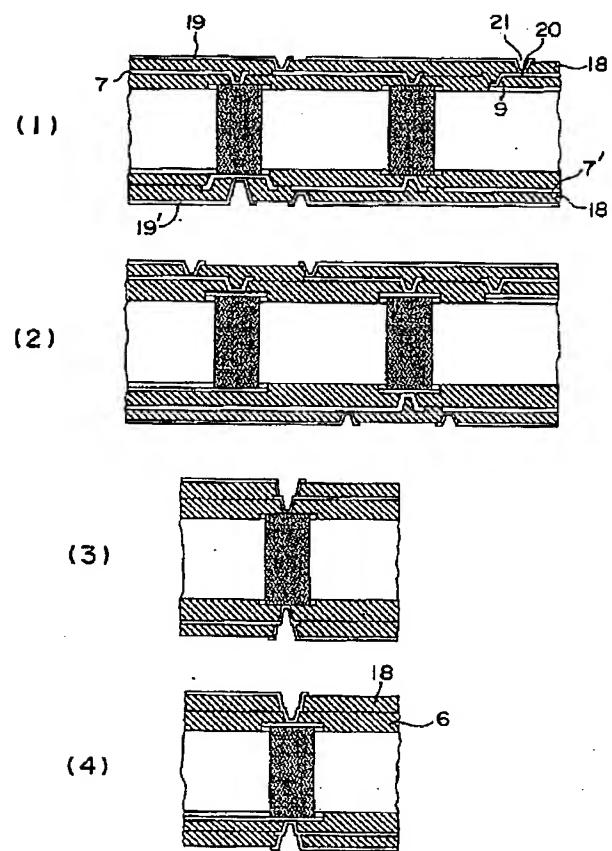
[Drawing 10]

図 9



## [Drawing 13]

図 1 1



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WRITTEN AMENDMENT

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## [Written amendment]

[Filing date] August 2, Heisei 5

[Amendment 1]

[Document to be Amended] Specification

[Item(s) to be Amended] Brief explanation of the drawings

[Method of Amendment] Change

[Proposed Amendment]

[Brief Description of the Drawings]

[Drawing 1] It is a sectional view showing one example of the multilayered circuit board of this invention.

[Drawing 2] It is a sectional view showing one conventional example of a multilayered circuit board.

[Drawing 3] It is a sectional view showing one conventional example now [ of a multilayered circuit board ].

[Drawing 4] It is a sectional view of a multilayered circuit board showing one conventional example now further.

[Drawing 5] It is a sectional view showing one example now [ of the multilayered circuit board of this invention ].

[Drawing 6] They are a series of sectional views showing one example of the manufacturing process of the multilayered circuit board of this invention.

[Drawing 7] They are a series of sectional views showing one example now [ of the manufacturing process of the multilayered circuit board of this invention ].

[Drawing 8] They are a series of sectional views showing the manufacturing process of the double-sided circuit board used for the manufacturing process of drawing 6.

[Drawing 9] They are a series of sectional views showing the manufacturing process of the double-sided circuit board used for the manufacturing process of drawing 7.

[Drawing 10] It is a figure showing the pattern for spalling tests according to JIS C-5012 to the multilayered circuit board of this invention.

[Drawing 11] It is a sectional view which illustrates the multilayered circuit board of this invention which has a circuit pattern of three layers on one side.

[Drawing 12] It is a figure showing the pattern for spalling tests according to JIS C-5012 to the multilayered circuit board of this invention.

[Drawing 13] It is a sectional view which illustrates the multilayered circuit board of this invention which has a circuit pattern of three layers on one side.

[Description of Notations]

1 Insulating substrate

2 The 1st layer circuit pattern

The 2' 1st layer circuit pattern

4 Conductive substance

5 Double-sided circuit board

6 Insulating layer

7 The 2nd layer circuit pattern

The 7' 2nd layer circuit pattern

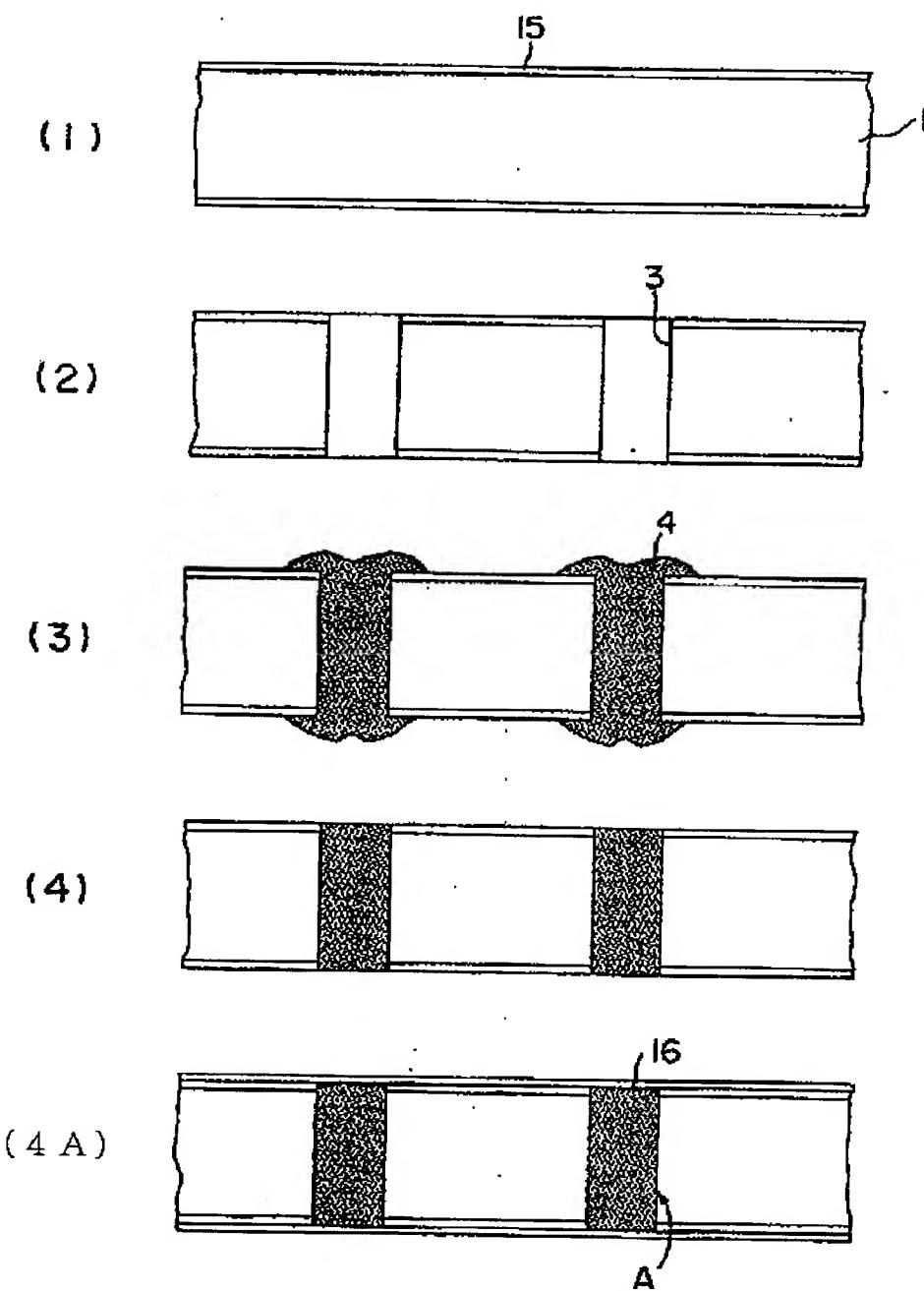
8 Opening

8' opening

9 The terminal area of a pattern

10 Metal skin  
11 Land  
12 Metal skin  
12' metal skin  
13 Terminal area  
14 Metal skin  
15 Conductive layer  
16 Metal skin  
17 Etching resist  
101 Prepreg  
102 Common through hole  
103 Through hole  
104 Circuit pattern  
105 Double-sided circuit board  
105' double-sided circuit board  
106 Insulating substrate  
107 Insulating layer  
108 The 1st layer circuit pattern  
109 The 2nd layer circuit pattern  
The 109' 3rd layer circuit pattern  
[Amendment 2]  
[Document to be Amended]DRAWINGS  
[Item(s) to be Amended]Drawing 8  
[Method of Amendment]Change  
[Proposed Amendment]  
Drawing 8

図 8



[Amendment 3]

[Document to be Amended] DRAWINGS

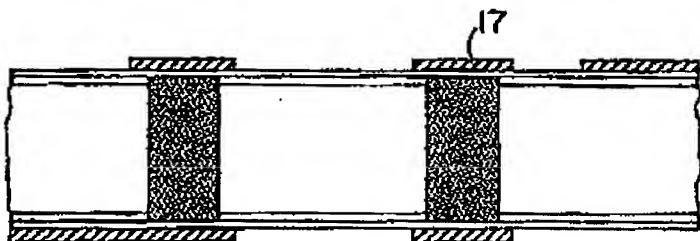
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[Method of Amendment] Change

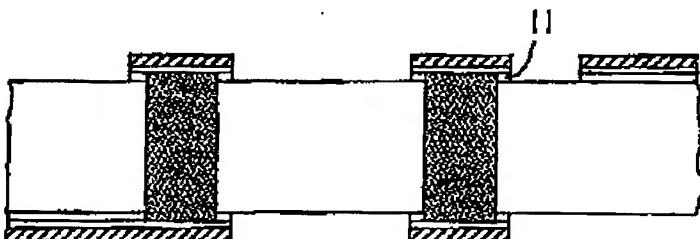
[Proposed Amendment]

[Drawing 9]

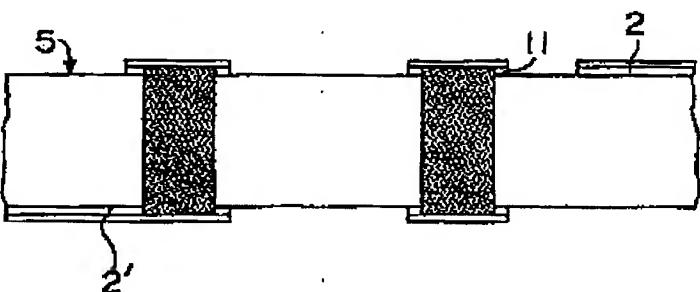
(5)



(6)



(7)



[Amendment 4]

[Document to be Amended] DRAWINGS

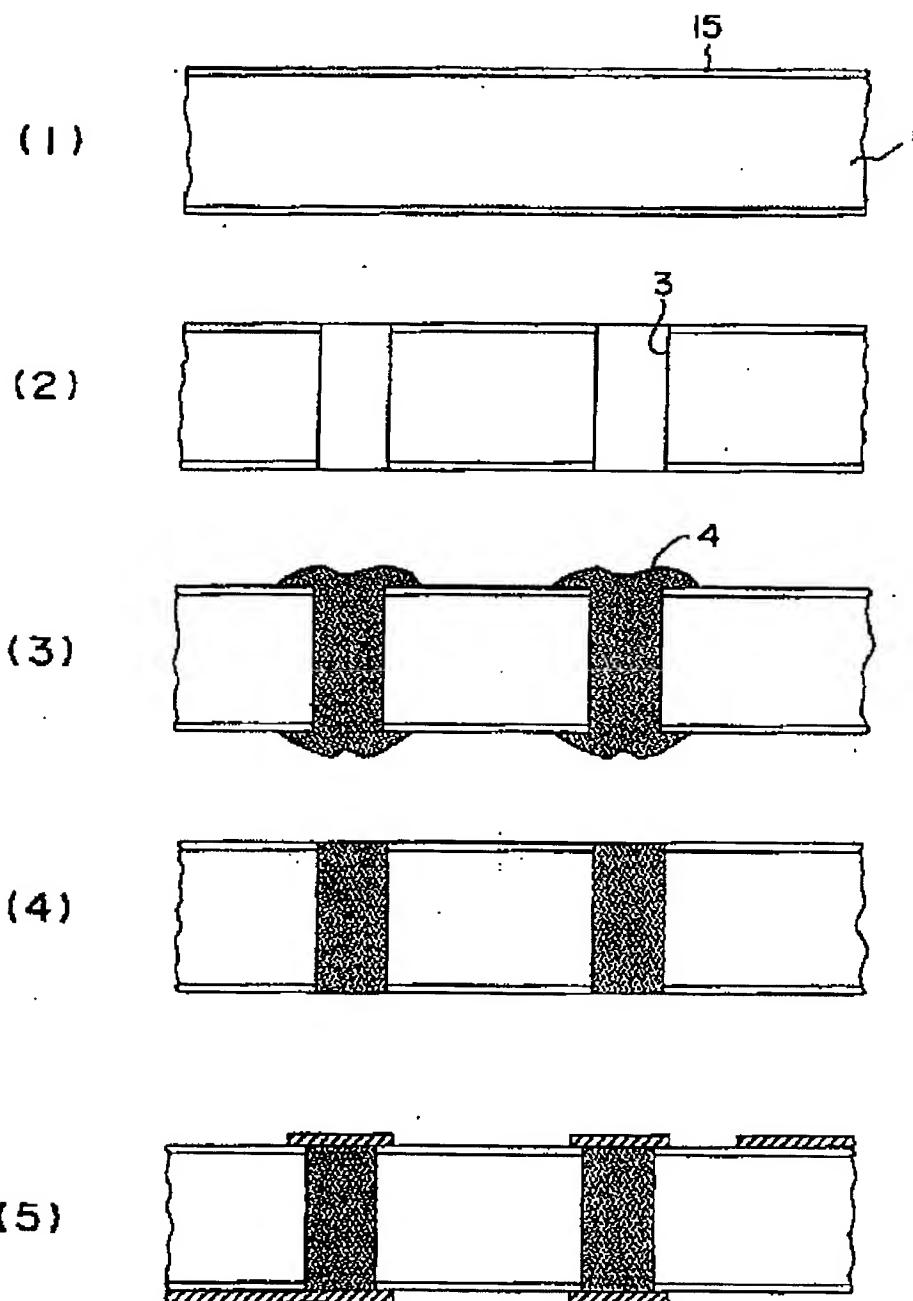
[Item(s) to be Amended] Drawing 10

[Method of Amendment] Change

[Proposed Amendment]

[Drawing 10]

## 図 10



[Amendment 5]

[Document to be Amended] DRAWINGS

[Item(s) to be Amended] Drawing 11

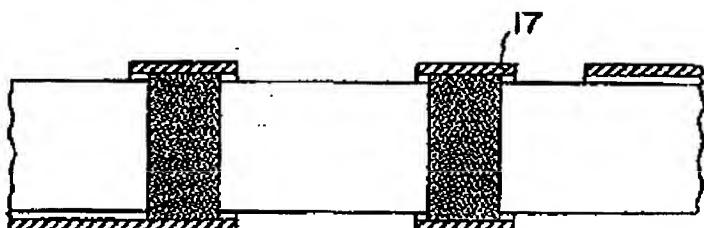
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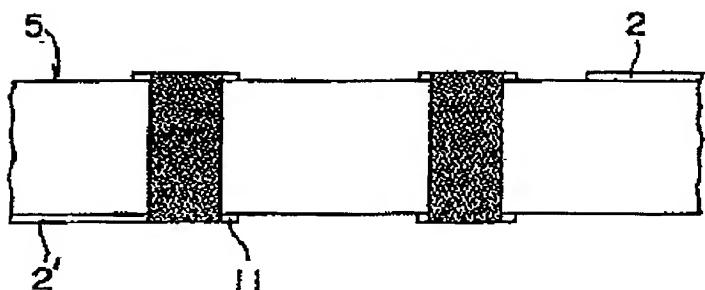
[Drawing 11]

図 1 1

(6)



(7)



[Amendment 6]

[Document to be Amended]DRAWINGS

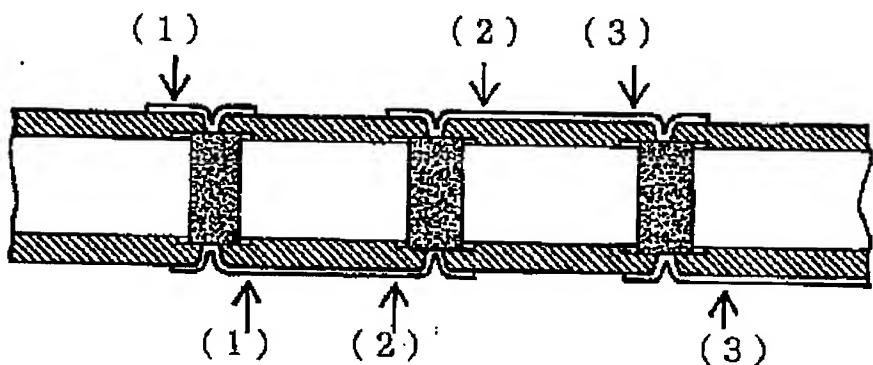
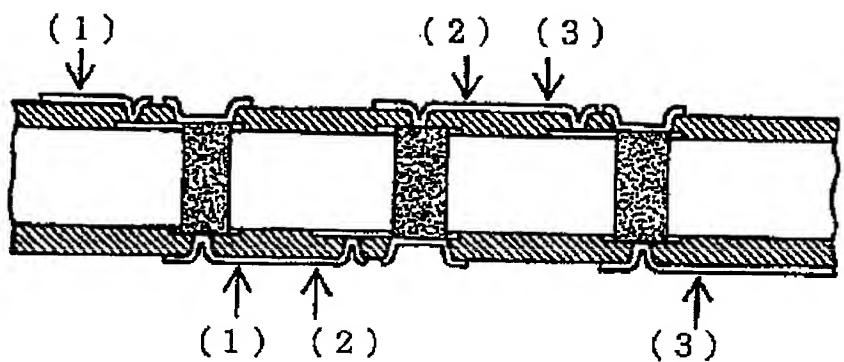
[Item(s) to be Amended]Drawing 12

[Method of Amendment]Change

[Proposed Amendment]

[Drawing 12]

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[Amendment 7]

[Document to be Amended] DRAWINGS

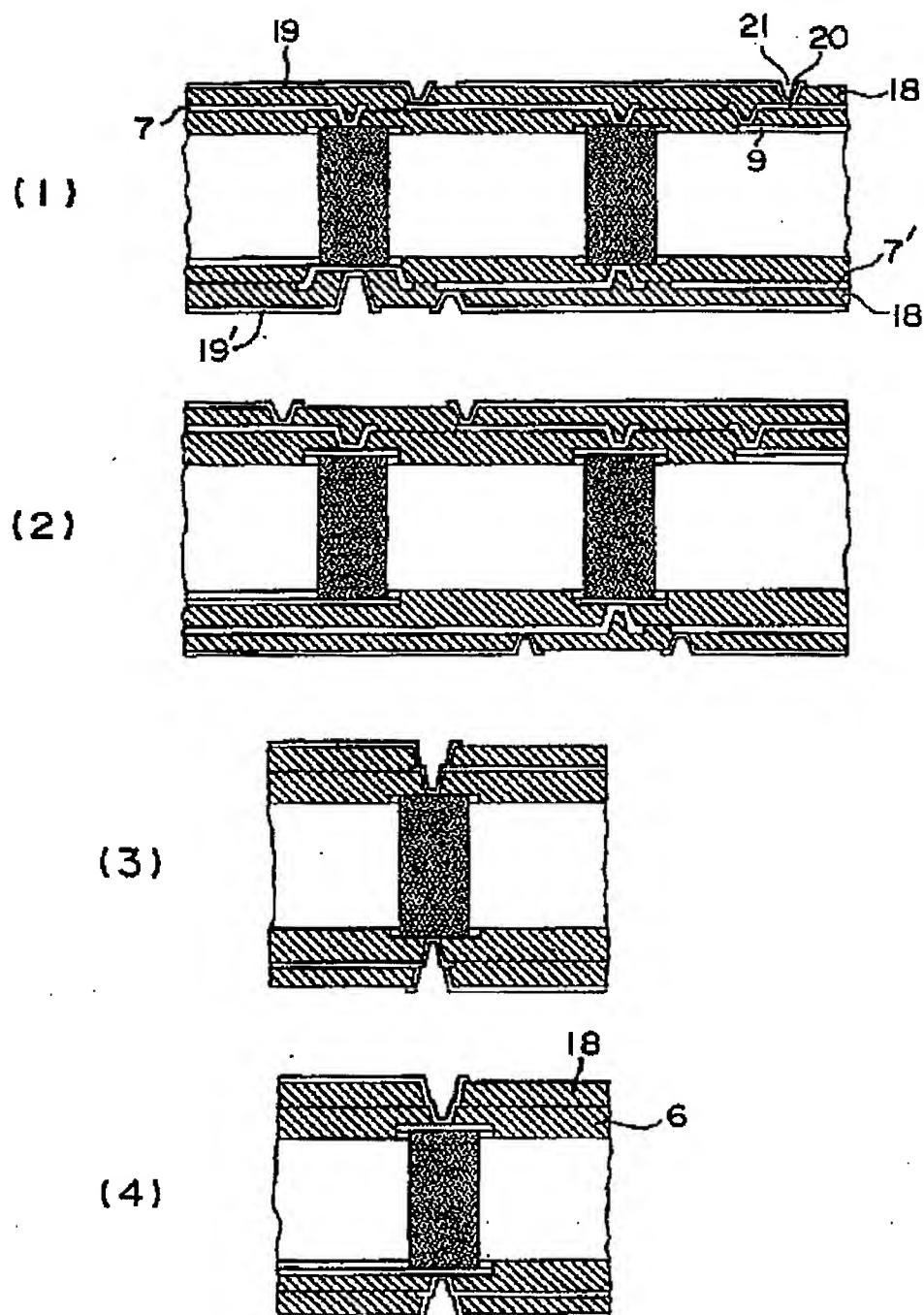
[Item(s) to be Amended] Drawing 13

[Method of Amendment] Change

[Proposed Amendment]

[Drawing 13]

図 1 3



[Translation done.]

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3. Detailed info of application
  - \* Kind of examiner's decision
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(21)出願番号	特願平5-96208	(71)出願人	000003182 株式会社トクヤマ 山口県徳山市御影町1番1号
(22)出願日	平成5年(1993)4月22日	(72)発明者	伊藤 順一 山口県徳山市御影町1番1号 徳山電通株式会社内
(31)優先権主張番号	特願平4-107984	(72)発明者	島本 敏次 山口県徳山市御影町1番1号 徳山電通株式会社内
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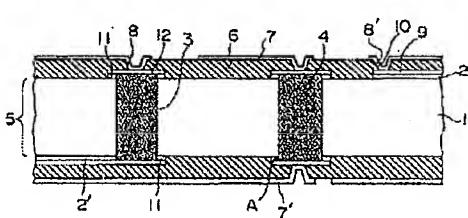
(54)【発明の名称】 多層回路基板及びその製造方法

(57)【要約】 (修正有)

【目的】 積層された各回路パターン間の電気的接続の信頼性を確保する。

【構成】 絶縁基板1の両面に形成された第1層回路パターン2、2'を有し、且つ該絶縁基板を貫通する貫通孔3に導電性物質4を充填し、該充填物の端面が第1層回路パターン2、2'の表面とほぼ同一平面になるように加工して形成されたスルーホール部Aを有する、表面が平坦な両面回路基板5を含む両面回路基板5の表裏両面に、絶縁層6を介してメッキ層からなる第2層回路パターン7、7'が形成され、また、連続したメッキ層10によって、第2回路パターン7、7'ヒスルーホール部Aとの間の電気的接続及び、第1層回路パターンと第2層回路パターンとの間の電気的接続が達成された多層回路基板である。

図 1



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## 【特許請求の範囲】

【請求項1】絶縁基板の両面に設けられた第1層回路パターンを有し、且つ絶縁基板を貫通する貫通孔に導電性物質を充填し、該充填物の端面が該第1層回路パターンの表面とほぼ同一平面になるように形成されたスルーホール部を有する、表面が平坦な両面回路基板及び該両面回路基板の少なくとも一方の表面に絶縁層を介して設けられたメッキ層からなる第2層回路パターンを含む多層回路基板であって、該第2層回路パターンと該スルーホール部との間の電気的接続は、該スルーホール部の端面の少なくとも一部が露出するように、該絶縁層に開口を形成し、該開口の内壁及び前記スルーホール部の端面の露出部を、第2層回路パターンのメッキ層と連続するメッキ層で被覆することにより成された多層回路基板。

【請求項2】絶縁基板の両面に設けられた第1層回路パターンを有し、且つ絶縁基板を貫通する貫通孔に導電性物質を充填し、該充填物の端面が該第1層回路パターンの表面とほぼ同一平面になるように形成されたスルーホール部を有する表面が平坦な両面回路基板を作製し、該両面回路基板の少なくとも一方の表面上に、該スルーホール部の端面の少なくとも一部が露出するように開口が形成された絶縁層を設け、該絶縁層の外表面、該開口の内壁及び前記スルーホール等の端面の露出部を連続するメッキ層で被覆し、該メッキ層の所定箇所をエッチングして第2層回路パターンを形成することからなる多層回路基板の製造方法。

## 【発明の詳細な説明】

## 【0001】

【産業上の利用分野】本発明は、絶縁基板上に、絶縁層を介して複数の回路パターンが形成された、プリント配線板として使用される、多層回路基板及びその製造方法に関する。

## 【0002】

【従来の技術】絶縁基板上に回路パターンを形成した回路基板において、1つの回路基板あたりの配線の密度を高くし、多機能化或いはコンパクト化を図る目的で、インターフェイシャルバイアホールを有する多層回路基板や、絶縁基板上に、絶縁層を介して複数の回路パターンが積層された多層回路基板が種々開発され、提案されている。

【0003】従来より知られている代表的な多層回路基板としては、例えば、次の様なものがある。なお、以下の説明において「両面回路基板」とは、基板の表裏両面に各1層の回路パターンが設けられた回路基板を意味する。

【0004】(1) PRINTED CIRCUITS HANDBOOK (第3版; 1988年発行) の a href="http://www.electronics.com/handbook/chapter33.html#33.2">http://www.electronics.com/handbook/chapter33.html#33.2 には、図2に示すように、両面に回路パターン104を有し、且つ貫通孔をメッキすることにより形成されたスルーホール103を

有する両面回路基板105及び105'が接着性樹脂によりなるプリプレグ101を介して積層され且つ全層を貫通するスルーホール102を形成することにより積層された両面回路基板の回路パターン相互の接続を行った多層回路基板が記載されている。

【0005】(2) 電子材料(1991年4月号)の103~108頁には、図3に示すように、絶縁基板106上に第1層回路パターン108が形成され、該回路パターン上に絶縁層107及び107'を介してメッキ層から形成した第2層回路パターン109及び第3層回路パターン109'が順次形成され、更に第4層又はそれ以上の回路パターンが形成され、且つ全層を貫通するスルーホール102を形成して最外層に電源層110を接続した多層回路基板が記載されている。

【0006】(3) 日本公開実用新案公報16482/1988には、図4に示すように、絶縁基板106上にメッキ層が形成した第1層の回路パターン108が形成され、該第1層の回路パターン上に絶縁層107及び107'を介してメッキ層から形成した回路パターン109及び109'が順次形成され、回路パターン間の絶縁層には、導電ペーストが絶縁体層と同一表面となるように充填されたインターフェイシャルバイアホール111が設けられ、これにより回路パターン間の電気的接続が成された回路基板が提案されている。

## 【0007】

【発明が解決しようとする課題】上記の内、(1)に示す多層回路基板は、現在実用化されているボリューラーなものであるが、かかる多層基板においては、別個に製造された複数の両面回路基板105及び105'をプリプレグ101を介して積層するため、回路基板間の位置合わせに極めて高い精度を要求される。即ち、複数の回路基板を積層後、全層を貫通して設けるスルーホール102が、各層の回路パターンにおいて確実に所定の箇所を貫通していることが必要であり、かかる積層の位置が狂うと直ちに不良が発生する。そのため、各回路パターンにおいて、該貫通部をある程度余裕を持たせて確保する必要があり、配線の高密度化に障害となっていた。また、全層を貫通するスルーホール102によってこのスルーホールと中間層に位置する回路パターンとの間の導通を行なう場合には、両端の接触面積が小さく、電気的接続の信頼性において問題があった。また、導通を必要としない回路パターンにもスルーホールが設けられるため、配線の自由度が制限され、このことによっても配線の高密度化が阻害されていた。

【0008】更に、上記多層回路基板は、単位回路基板の製造工程において最低2回のメッキを必要とするのみならず、単位回路基板の積層工程、積層後の孔明け、メッキ等を必要とし、製造上においても、極めて複雑であった。

【0009】(2)に示す多層回路基板も、全層を貫通

(3)

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してスルーホール102を設けるものであり、上記(1)の多層回路基板と同様、配線密度の高密度化に障害となっていた。また、回路パターンは絶縁基板の片面のみに積層されるものであり、回路パターンの層数の増加に伴う回路パターン間の電気的接続端子の数の増加の程度が大きくこれによっても配線の高密度化が阻害されていた。

【0010】更に、上記多層回路基板の製造においては、回路パターンを1層形成するために絶縁層の形成及びメッキをそれぞれ1回行う必要があり、また、全回路パターンを形成後も、孔明け、メッキ等を必要とし、製造上においても改善の余地があった。

【0011】(3)に示す多層回路基板は、絶縁層を介して積層された複数の回路パターンを、該絶縁層に設けられた開口に導電ペーストを充填することにより接続するものである。ところが、該開口は貫通孔とは異なり、穴の底が塞がっているため、これに充填されて硬化された導電ペーストは、硬化時の収縮によって接触する回路パターン面との間に空隙ができ易く、かかる部分の電気的接続の信頼性において改良の余地がある。また、上記(2)と同様、回路パターンは絶縁基板の片面のみに積層されるものであり、回路パターンの層数の増加に対する回路パターン間の電気的接続端子の数の増加の程度が大きく、これによって配線の高密度化が阻害されていた。

【0012】更に、上記多層回路基板の製造においては、絶縁層及び開口に充填された導電ペーストの硬化を各層毎に別々に行うことが必要であり、回路パターン間を1回接続する毎に2回もの熟履歴を受け、製造工程が複雑化するばかりでなく、基板自体の熱による劣化の問題が生じる。

【0013】また、上記(2)、(3)の多層回路基板においては、電子部品の実装も片面に限られるため、実装密度の低下をも招いていた。

【0014】従って、本発明の目的は、上述した従来の問題点を解消し、積層された各回路パターン間の電気的接続の信頼性が高く、配線の高密度化が達成され、且つ部品の実装密度の高密度化が可能な多層回路基板及びその製造方法を提供することにある。

【0015】

【課題を解決するための手段】本発明者らは、上記した目的を達成すべく鋭意研究を重ねた。その結果、絶縁基板の両面に第1層の回路パターンを形成すると共に、該絶縁基板を貫通する貫通孔に導電性物質を充填してスルーホール部を形成することにより作成した表面が平坦化された両面回路基板を使用することにより、該両面回路基板上に絶縁層の形成及びメッキ層からの回路パターンの形成が極めて高精度で行えること、また、該両面回路基板の両面に絶縁層を介してメッキ層を形成し、このメッキ層により、回路パターンの形成、および回路パターン間或いは回路パターンとスルーホール部の電気的接続

を行うことにより、全層に貫通するスルーホール部を別途設けることなく、自由度の高い回路パターンを形成することができるため、配線の高密度化が図れること、更には、両面回路基板の両面に回路パターンを積層するため、電子部品を両面に実装できることを見い出した。また、製造工程においては、両面回路基板の両面に回路パターンを積層することができるため、絶縁層の形成、メッキ層の形成、該メッキ層から回路パターン形成のための処理を両面同時に行うことができ、製造工程の効率化を図ることを見い出した。

【0016】即ち、本発明は、絶縁基板の両面に設けられた第1層回路パターンを有し、且つ絶縁基板を貫通する貫通孔に導電性物質を充填し、該充填物の端面が該第1層回路パターンの表面とほぼ同一平面になるように形成されたスルーホール部を有する、表面が平坦な両面回路基板、及び該両面回路基板の少なくとも一方の表面に絶縁層を介して設けられたメッキ層からなる第2層回路パターンを含む多層回路基板であって、該第2層回路パターンと該スルーホール部との間の電気的接続は、該スルーホール部の端面の少なくとも一部が露出するよう、該絶縁層に開口を形成し、該開口の内壁及び前記スルーホール部の端面の露出部を、第2層回路パターンのメッキ層を連続するメッキ層で被覆することにより成された多層回路基板を提供する。

【0017】更に、本発明は上記多層回路基板の製造方法として、絶縁基板の両面に設けられた第1層回路パターンを有し、且つ絶縁基板を貫通する貫通孔に導電性物質を充填し、該充填物の端面が該第1層回路パターンの表面とほぼ同一平面になるように形成されたスルーホール部を有する表面が平坦な両面回路基板を作製し、該両面回路基板の少なくとも一方の表面上に、該スルーホール部の端面の少なくとも一部が露出するよう、開口が形成された絶縁層を設け、該絶縁層の外表面、該開口の内壁及び前記スルーホール部の端面の露出部を連続するメッキ層で被覆し、該メッキ層の所定箇所をエッチングして第2層回路パターンを形成する方法を含む多層回路基板の製造方法をも提供する。

【0018】本発明の代表的な態様の多層回路基板の断面図を図1および図5に示す。

【0019】上記の図面に示すように、本発明の多層回路基板は、絶縁基板1の両面に形成された第1層回路パターン2、2'を有し、且つ該絶縁基板を貫通する貫通孔3に導電性物質4を充填し、該充填物の端面が第1層回路パターン2、2'の表面とほぼ同一平面になるように加工して形成されたスルーホール部Aを有する、表面が平坦な両面回路基板5を含む。両面回路基板5の表裏両面に、絶縁層6を介してメッキ層からなる第2層回路パターン7、7'が形成されている。絶縁層6には、スルーホール部Aの端面の一部を露出するよう開口8が設けられており、また絶縁層6には、第1層回路パター

ン2の端子部9の一部を露出するように別の開口8'も設けられている。絶縁層6の外側面、開口8及び8'の内壁、スルーホール部の露出面及び端子部9の露出面にわたって連続したメッキ層を被覆し、そして絶縁層6上のメッキ層の所要箇所をエッチングすることにより第2層回路パターン7、7'が形成される。また上記連続したメッキ層によって、第2層回路パターン7、7'とスルーホール部Aとの間の電気的接続及び、第1層回路パターンと第2層回路パターンとの間の電気的接続が達成される。

【0020】上記絶縁基板1として、公知の材質、構造を有するものが制限なく使用される。代表的なものを例示すれば、紙基材-フェノール樹脂積層基板、紙基材-エポキシ樹脂積層基板、紙基材-ポリエステル樹脂積層基板、ガラス基材-エポキシ樹脂積層基板、紙基材-テフロン樹脂積層基板、ガラス基材-ポリイミド樹脂積層基板、ガラス基材-BT(ビスマレイミドートリアジン)レジン樹脂積層基板、コンポジット樹脂基板等の合成樹脂基板や、ポリイミド樹脂、ポリエステル樹脂等のフレキシブル基板や、貫通孔を設けたアルミニウム、鉄、ステンレス等の金属板をエポキシ樹脂等で覆って絶縁処理した金属系絶縁基板、あるいはセラミックス基板等が挙げられる。

【0021】また、絶縁基板1の両面に形成される第1層の回路パターン2、2'の材質は、導電性を有する公知の材質が特に制限なく使用できる。代表的な材質を例示すれば、銅、ニッケル、アルミニウム等が挙げられる。そのうち、銅が最も好適に使用される。また、上記回路パターンの厚みについても特に制限されないが、一般には5~70μmが適当である。

【0022】上記両面回路基板において、スルーホール部Aは、絶縁基板の所定の箇所に絶縁基板を貫通して設けられた貫通孔3に導電性を有する充填物4をその端面が平滑で且つ両面回路基板の両表面とほぼ同一平面をなすように充填して形成される。かかる導電性を有する充填物は、公知の材質が特に制限なく使用される。例えば、導電性を有する硬化体を与える硬化性導電物質の硬化体が代表的である。該硬化性導電物質として、金、銀、銅、ニッケル、鉛、カーボン等の導電材料とエポキシ樹脂、フェノール樹脂等の公知の架橋性の熱硬化性樹脂などを必要により有機溶剤と共に混合してペースト状とした公知の硬化性導電物質を使用することができる。

【0023】また、上記硬化性導電物質は、良好な導電性を有するスルーホール部を形成するために、硬化後の電気抵抗が、 $1 \times 10^{-2} \Omega \cdot \text{cm}$ 以下となるように、導電材料の選択、及び各成分の使用量を調節することができる。

【0024】更に、スルーホール部の径は、特に制限されるものではなく、任意に設定することができる。一般には、前記硬化性導電物質を充填することが可能な程度

の孔径以上であればよく、具体的には、0.2mm以上、好ましくは、0.3~2mmの範囲である。

【0025】上記のスルーホール部の形成において、貫通孔3に充填する導電性を有する充填物の最外層をメッキ層によって形成すると、スルーホール部の電気的信頼性を一層高めることができる。

【0026】また、上記両面回路基板の第1層回路パターン2、2'とスルーホール部Aとの電気的接続は、該第1層回路パターンにおいて該スルーホール部Aの周囲にランド部11を設けることによって行うのが好適である。この場合、ランド部とスルーホール部との電気的接続をより向上させるために、ランド部とスルーホール部の端面を連続したメッキ層12によって被覆することが好ましい。かかるメッキ層12は、図1に示すように独立して設けても良いし、図5に示すように積層された回路パターン7、7'を構成するためのメッキ層を利用しても良い。

【0027】本発明において、上記両面回路基板5の少なくとも一方の表面には、絶縁層6を介して形成されるメッキ層よりなる回路パターン7、7'が1層以上形成される。

【0028】上記絶縁層6としては、公知の材質よりもがとくに制限なく使用される。例えば、感光性絶縁レジストとして知られている公知の硬化性絶縁樹脂、例えば、プロピマー52(商品名:チバガイギー社製)、プロピコート5000(商品名:日本ペイント社製)等が好適である。また、絶縁層の厚みは、その両面に存在する回路パターン間の絶縁性を維持し得る程度であればよく、一般には、20~100μmの厚みが適当である。

【0029】上記絶縁層表面は、表面に形成されるメッキ層の密着性を向上させるため、粗面化処理を施すことが好ましい。粗面化処理の方法は、バフ、ブラシ等で物理的に研磨する方法、アルカリ性過マンガン酸カリウム溶液、クロム酸溶液に浸漬することにより化学的に粗面化する方法などの公知の方法が特に制限なく採用される。

【0030】また、回路パターンを構成するメッキ層も公知の材質がとくに制限なく使用される。例えば、銅、ニッケル等が挙げられる。そのうち、銅が最も好適に使用される。上記メッキ層の厚みは、導電性を発揮し得る程度の厚みが確保されればよく、通常50μm以下の厚み、好ましくは5μm~35μm程度の厚みが好適である。

【0031】本発明において、絶縁層6には、形成された回路パターン間または回路パターンとスルーホール部を接続するための開口8が存在する。かかる開口は、回路パターンの端子部、或いはスルーホール部の端面の少なくとも一部を露出するように設けられる。回路パターン同志を接続する場合には、両面回路基板に近い側の回

路パターンの端子部を露出するように開口8が形成される。かかる露出面積は、後で述べるメッキ層10の被覆により電気的接続が達成される程度でよい。一般には、絶縁層より露出する部分の面積は、相当径50μmφ以上の面積で露出すればよい。更にまた、開口の形状は特に限定されず、円形、橢円形、長方形、正方形等、回路パターンの設計に適した形状を適宜採用すればよい。

【0032】尚、図5に示すように、該スルーホール部Aの周囲に第1層回路パターンのランド部11を設けるがこれらの表面にメッキ層が形成されていない場合は、スルーホール部の端面の金属面を露出させ、更に該ランド部を含む面積まで露出させることが望ましい。そして、該開口の内壁と該開口によって露出した第1層回路パターンのランド部及びスルーホール部とを、積層された回路パターンのメッキ層と連続するメッキ層によって被覆する。例えば、図5においては、開口8によって露出した第1層回路パターン2'のランド部11とスルーホール部Aの端面とを、回路パターン7'を構成するメッキ層と連続するメッキ層12'によって被覆する構造が示されている。

【0033】また、第1層回路パターン2'とスルーホール部Aの端面との電気的接続は、上記回路構造以外に、例えば、スルーホール部の端面の一部と第1層配線パターンの端子部とが露出するように絶縁層に開口を形成し、該露出部及びその間の絶縁層を連続するメッキ層により被覆する態様によって行うことも可能である。

【0034】本発明の多層回路基板の他の構造として公知の多層基板の構造がとくに制限なく採用される。例えば、図には示されていないが、最外層の必要所望の箇所に、ソルダーレジストによる耐性の良好な層を設けることが好ましい。

【0035】図1および図5に示した態様の多層回路基板は、両面回路基板の両面に存在する第1層回路パターン上にそれぞれ絶縁層を介して1層の回路パターンを形成した4層回路基板の例を示したが、本発明はこれに限定されるものではなく、該回路パターン上に絶縁層を介して更に回路基板を積層した構造も可能である。このような例は図11(1)～(4)に示されている。

【0036】即ち、図11は、第2層回路パターン7'、7の表面に絶縁層18を介して、メッキ層よりも第3層回路パターン19、19'が形成されたいくつかの実施態様を示す。図11の(1)は、図5に示す態様の多層回路基板の第2の回路パターン上に第3層回路パターンを形成した態様である。また、図11の(2)は、図1に示す態様の多層回路基板の第2の回路パターン上に第3層回路パターンを形成した態様である。更に、(3)、(4)に示す態様は、スルーホール部の位置に、該スルーホール部と順次接続する第2層回路パターン、第3層回路パターンが存在する態様、或いはスルーホール部に第3層回路パターンを第2層回路パターン

を介すことなく直接接続した態様を示す。

【0037】これらの態様において、絶縁層18および第3層回路パターンの形成及び他層或いはスルーホール部との電気的接続は、前記絶縁層6および第2層回路パターンの形成方法に準じて行われる。

【0038】例えば、第3層回路パターンの形成は、所定の箇所に開口を形成する絶縁層を形成した後、メッキ層を形成し、所定の箇所をエッチングする事によって行われる。また、第3層回路パターンと他の回路パターン、スルーホール部との電気的接続は、第1層回路パターンの端子部9、第2層回路パターンの端子部20またはスルーホール部Aの端面の少なくとも一部が露出するよう絶縁層18に開口21を設け、第3層回路パターン19、19'を形成するメッキ層と連続するメッキ層によって、該開口の側面と該露出部とを被覆することによって第3層回路パターンと第2層回路パターン、第1層回路パターン若しくはスルーホール部とを接続することができる。

【0039】尚、上記接続において、第3層回路パターンと第1層回路パターン或いはスルーホール部とを直接接続する場合は、(4)に示すように絶縁層6及び絶縁層18に順次開口を設け、前記メッキ層による被覆を行えば良い。

【0040】本発明の多層回路基板の代表的な製造方法を例示すれば、以下の方法が挙げられる。

【0041】即ち、図6は、多層回路基板を製造する工程を断面図で示したものである。かかる図に示すように、(1)絶縁基板1の両面に第1層回路パターン2、2'を有し、且つ該絶縁基板を貫通する貫通孔3を有し、該貫通孔に導電性を有する充填物4を充填してスルーホール部Aが形成された表面が平坦な両面回路基板5の少なくとも一方の表面に、(2)上記の第1層回路パターン上に形成される第2層回路パターンと接続が必要な第1層回路パターンの端子部13とスルーホール部Aとを露出させる開口8を形成するよう絶縁層6で被覆した後、(6)該露出部及び開口8の内壁及び絶縁層表面をメッキ層14で被覆し、(4)該メッキ層の所定箇所をエッチングして回路パターンを形成することにより、第2層以上の回路パターン7、7'および該回路パターンに連続する導通用のメッキ層10を形成する。

【0042】上記絶縁層6の形成方法は、特に限定されず、公知の方法が制限なく採用される。一般には、ドライフィルム、液状レジスト、ドライフィルム・液体レジスト併用等の種々の形態の光或いは熱により硬化する硬化性絶縁樹脂を使用することができる。該絶縁層の形成方法としては、上記硬化性絶縁樹脂を使用し、印刷法、写真法等の方法をファイン度に従って適宜選択して採用すればよい。例えば、光の照射により硬化する液状レジスト、ドライフィルム等の硬化性絶縁樹脂層を両面回路基板の全面に積層し、開口の形成が必要な箇所を除いて

光を照射後、未硬化部分を現像により除去することによって絶縁層を形成することができる。

【0043】上記の方法で、絶縁層の形成に光により硬化するドライフィルムを用いると、絶縁樹脂層の厚み精度もよく、表・裏面同時に形成することもできるため、より効率的に且つ高精度で絶縁層を形成することができる。

【0044】また、図6に示す態様において、上記絶縁層6の開口8の大きさは、メッキ層により電気的接続が得られる前記範囲の大きさとすることが好ましい。

【0045】図7は図6に示す態様に対して、メッキ層12を形成していない両面回路基板を使用する態様を示すものである。この場合、第1層回路パターン2' と電気的接続の必要なスルーホール部Aとの導通を確実にするため、絶縁層6に設ける開口8は、該スルーホール部Aの端面の全面積とその周囲の回路パターンのランド部11とが露出するように設けられる。このようにすることにより、統くメッキ層14の形成により露出部分が同時にメッキされ、該部分の電気的接続を確実に行うことができる。

【0046】また、上記図7に示す工程によると、図6に示す工程よりメッキ工程を1工程減らすことも可能である。

【0047】前記方法において、メッキ層14の形成する方法は特に制限されないが、一般には、金属の無電解メッキ法が好適である。

【0048】また、メッキ層から回路パターンを形成するためには、前記第1層回路パターンの形成と同様な方法を適用することができる。一般的にエッチング法が好適である。

【0049】また、本発明においては、第2層の回路パターン上に同様にして、更に、絶縁層及び回路パターンを順次積層することも可能である。

【0050】上記の積層される回路パターンは、信号線、電源線、グラウンド線、電磁波シールド層に特に制限されずに用いられる。

【0051】尚、図6では両面回路基板のスルーホール部Aの端面が予めメッキ層12によって被覆された態様を示したが、かかるメッキ層は必須のものではない。

【0052】また、該メッキ層を形成しない場合は、図7に示すように第2層回路パターンの形成時に、この回路パターンのメッキ層に連続するようにメッキ層を設けて形成しても良い。即ち、図7においては、第1層回路パターンと接続する必要のあるスルーホール部Aの端面及びその周囲に形成された第1層回路パターンのランド部11とが絶縁層6の開口により露出するように該絶縁層を形成し、統くメッキ層14の形成時に該露出部分を同時にメッキを行う態様を示す。

【0053】上記製造方法において、両面回路基板の具体的な製造方法は、とくに制限されるものではなく、得

られる多層回路基板の構造に応じて適宜決定すれば良い。かかる両面回路基板の製造方法を例示すれば、例えば前記図6に示す製造工程に使用する両面回路基板は、図8に示す方法が、また、前記図7に示す製造工程に使用する両面回路基板は、図9に示す方法が代表的な方法として挙げられる。

【0054】即ち、図8においては、両面に導電層15を有する絶縁基板1にスルーホール用の貫通孔3を設け、該貫通孔に導電性を有する硬化体4を与える硬化性導電物質を、硬化後に該硬化体が貫通孔から突出するよう充填して硬化させ、該導電層及び硬化体によって構成される表面がほぼ同一平面になるように平滑に研磨して前記導電層面にスルーホール部Aを形成した後、該平滑化された表面にメッキ層16を設け、該導電層及びメッキ層よりなる導電体層の所定箇所をエッチングして第1層回路パターン2、2'を形成することにより両面回路基板を得る態様が示されている。図9においては、両面に導電層15を有する絶縁基板1にスルーホール用貫通孔3を設け、該貫通孔に導電性を有する硬化体4を与える硬化性導電物質を、硬化後に該硬化体が貫通孔より突出するよう充填して硬化させ、該導電層及び硬化体によって構成される面がほぼ同一平面になるように平滑に研磨して前記導電層間にスルーホール部Aを形成した後、上記導電層の所定箇所をエッチングして第1層回路パターン2、2'を形成することにより両面回路基板を得る態様が示される。

【0055】以下、上記工程を更に詳細に説明する。

【0056】絶縁基板1の両面に導電層を設けた原料基板は、絶縁基板上に銅等の金属層をメッキによって形成したもの、銅等の金属層を接着により張り合わせたものなど公知のものがとくに制限なく使用される。

【0057】両面に導電層を有する絶縁基板には、先ずスルーホール部形成のための貫通孔3が設けられる。上記貫通孔の径は、目的とするスルーホール部の径に対応する径を選択すれば良い。上記貫通孔3の形成方法としては、ドリリング加工、パンチング加工、レーザー加工等の通常の回路基板の製造と同様の公知の手段が特に限定されずに用いられる。この場合、貫通孔3に充填される硬化性導電物質の硬化体と導電層との電気的接続の信頼性を向上させるため、該貫通孔の周辺部に位置する導電層に傾斜面を存在させ、該硬化体との接触面積を増大させてもよい。上記の貫通孔における導電層の周辺部の少なくとも一部に傾斜面を存在させる方法は、両面に導電層を有する絶縁基板にスルーホール用の貫通孔を形成した後に、ソフトエッチング液によりソフトエッチングを行い該傾斜面を形成する方法、或いは、貫通孔を形成した後に、貫通孔よりも径の若干大きなドリルにより、導電層及び絶縁層をテープ上に研削する方法、貫通孔よりも少し大きな径を持つエッティングレジストを貫通孔周辺に形成し、エッティングを行い形成する方法等が特に限

(7)

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定されずに用いることができる。

【0058】両面回路基板のスルーホール部Aに存在する導電性を有する充填物は、上記硬化性導電物質を絶縁基板の貫通孔3に充填・硬化することによって形成することが好ましい。

【0059】硬化性導電物質の貫通孔への充填は、該硬化性導電物質が貫通孔の全空間を満たし、且つ導電層の両表面より若干、具体的には、0.05mm以上、好ましくは、0.1～2mm突出する程度に充填する方法が推奨される。かかる硬化性導電物質の代表的な充填法を例示すれば、印刷法によって1回或いは複数回の塗布を行なう方法、絶縁基板の表裏両側から表裏一対のスキーで圧入する方法、ロールコーラー或いはカーテンコーラーによって充填し、余分の塗料をスキーで掻き取る方法等の手段が好適に用いられる。

【0060】また、貫通孔に充填された硬化性導電物質の硬化は、熱風炉、赤外線炉、遠赤外線炉、紫外線硬化炉、電子線硬化炉等の公知の硬化方法より、硬化性導電物質の硬化に適するものを適宜選んで硬化させれば良い。

【0061】硬化性導電物質を硬化後、導電層の表面と硬化性導電物質の硬化体によって構成される表面とがほぼ同一表面になるように、両表面を平滑に研磨することが重要である。即ち、かかる研磨により、後工程である配線パターンの形成において、エッチングレジストによるパターンの形成、及びエッチングを精度良く行なうことができ、更に該配線パターン上への絶縁層をも信頼性よく形成することが可能となる。

【0062】導電層及び硬化性導電物質によって構成される表面を上述のように平滑に研磨する方法としては、スライヤー研磨、パフ研磨、スクラブ研磨等の通常の研磨に用いられる方法が一般に用いられる。

【0063】図8においては、スルーホール部Aを含む導電層15の平滑化された面上に、メッキ層16を形成する態様を示す。かかるメッキ層を形成し、且つ続くエッチングで該スルーホール部周辺にランド部11を形成するように導電層を残すことにより、第1層回路パターンを形成する前に、スルーホール部と回路パターンのランド部とを共通のメッキ層で被覆することができる。かかるメッキ層の形成によりスルーホール部による電気的信頼性が向上する。もちろん、上記メッキ層によるスルーホール部と回路パターンのランド部との被覆を、図7に閲覧して説明したように、絶縁層を介して第2層回路パターンを積層する際に行なうことも可能である。

【0064】上記メッキ層16の形成方法は、化学メッキ法或いは、電気メッキ法で行なうことができる。該メッキ層の材質は、公知の導電性金属が特に制限されずに用いられるが、一般には、前記導電性を有する硬化体を与える硬化性導電物質の材質として使用される銅等の導電性金属と同じ材質を選択するのが好ましい。また、メッ

キ層の厚みは、特に制限はされないが、通常50μm以下の厚みで、好ましくは5μm～35μm程度で行なうのがよい。

【0065】上記のように、スルーホール部分と導電層或いは導電層とメッキ層との平滑化された面には、図8及び図9の(5)から(7)の工程に示すように第1層回路パターンが形成される。

【0066】即ち、第1層回路パターンの形成方法は、エッチングレジスト17によりエッチングパターンを形成し、エッチングを行う方法が一般的である。ここで用いられるエッチングレジストはドライフィルム、レジストインク等が特に制限無く使用され、パターンのファイン度によって適宜選択して使用すればよい。また、エッチングレジストパターンはエッチング法によってポジパターン或いはネガパターンを適宜採用すればよい。例えば、テンディング法に代表されるエッチング法ではポジパターンを、半田剥離法、SES法に代表されるエッチング法ではネガパターンを採用すればよい。

【0067】

【発明の効果】以上のお説明より理解されるように、本発明によれば、絶縁基板の両面に第1層の回路パターンを形成すると共に、該絶縁基板を貫通する貫通孔に導電性物質を充填してスルーホール部を形成して構成された、表面が平坦化された両面回路基板を用い、該両面回路基板上に絶縁層の形成及びメッキ層による第2層回路パターンの形成を行うことにより、該積層される第2層回路パターンの形成を極めて高精度で行なうことができる。また、該両面回路基板の両面に絶縁層の形成とそれに続くメッキ層の形成により、回路パターンの形成と回路パターン間あるいは回路パターンとスルーホール部の電気的接続とを行なうことにより、全層に貫通するスルーホール部を別途設けることなく、高い自由度で回路パターンを形成することができるため、配線の高密度化を図ることが可能である。

【0068】更に、製造工程においては、両面回路基板の両面に回路パターンを積層することができるため、絶縁層の形成、メッキ層の形成、該メッキ層から回路パターン形成のための処理を両面同時に行なうことができ、製造工程の効率化を図ることができる。

【0069】更にまた、両面に回路パターンが形成されているため、電子部品を両面に実装することができる。

【0070】

【実施例】以下、本発明を具体的に説明するために実施例を示すが、本発明はこれらの実施例に限定されるものではない。

【0071】実施例1

図8に示す工程に従って両面回路基板を製造し、該両面回路基板を使用して図6に示す工程に従って多層回路基板を製造した。

【0072】即ち、図8に示すように(1)両面に導電

層1 5を有する絶縁基板1として、厚さ1.6mmのガラス基材エポキシ樹脂鋼張り積層板を使用して、(2)直径0.4mmの貫通孔3をドリル加工により設けた。

(3) 該貫通孔3に硬化性導電物質4として、市販の熱硬化性銀ペースト(徳力化研(株)社製、PS-652(商品名))を、その硬化体が貫通孔3より若干突出するようにスクリーン印刷法により充填した。該銀ペーストを熱風乾燥炉で80°Cで4時間、150°Cで2時間の条件で乾燥硬化して導電性を有する充填物4を構成した。(4) 次に320番及び600番のバフを順次使用して、硬化した銀ペーストの硬化体が突出した面を研削し、該硬化体を含む導電層表面を平滑化した。次いで、(4')スルーホール部Aを含む平滑化された導電層表面に、電気メッキを施した。メッキ浴は日本シェーリング(株)社製のカバラシドG S(商品名)を使用し、電流密度2A/dm<sup>2</sup>の条件で厚み10μmの銅メッキ層16を形成した。

【0073】次いで、(5)平滑化された導電層表面に、エッティングレジスト17としてドライフィルム(ハイキュレス(株)社製「アクリマーCF」1.5ml)をラミネートし、露光、現像してレジストパターンを形成した。その後、(6)塩化第2銅エッティング液でエッティングを行い、(7)エッティングレジストを剥離することによって、ランド部11を有する第1層配線パターン2、2'を有する両面回路基板5を得た。

【0074】次いで、図6に示すように、(1)上記両面回路基板5を使用して(2)スルーホール部Aを含む第1層配線パターン上に、絶縁層を形成するため、感光性絶縁レジスト(プロピコート5000:商品名、日本ペイント社製)を塗布、乾燥し、露光、現像を行った後熟硬化し、電気的接続を必要とする部分に絶縁層6の開口8を有するパターンを形成した。次に、(3)上記絶縁層表面を粗面化処理をした後、その両面に無電解メッキ、電解メッキを施し、厚み10μmの銅メッキ層14を形成した。次いで、(4)銅メッキ層14表面に、前記(5)で使用したエッティングレジスト17をラミネートし、露光、現像してレジストパターンを形成し、塩化第2銅エッティング液でエッティングを行った後、エッティングレジストを剥離することによって、配線パターン7、7'を形成して4層の回路パターンを有する多層回路基板を得た。

【0075】得られた多層回路基板の表裏に位置し、且つ共通するスルーホールに接続する配線パターン7、7'間の抵抗を測定した結果、31mΩであった。また、図10に示すような、多層回路基板の表裏に位置する該配線パターン7、7'間を含むテストパターンを使用したJIS C-5012の熱衝撃試験(-65°C×30分→125°C×30分)(図10において(1)-(1)、(2)-(2)及び(3)-(3)間の抵抗測定)において、サイクル数500回を過ぎても、上記

の多層回路基板の表裏に位置する該配線パターン7、7'間を含むテストパターンの導通があり、また、その後の電気的抵抗の上昇もほとんどなかった。

【0076】実施例2

図9に示す工程に従って両面回路基板を製造し、該両面回路基板を使用して図7に示す工程に従って多層回路基板を製造した。

【0077】即ち、図9に示すように(1)両面に導電層15を有する絶縁基板1として、厚さ1.6mmのガラス基材エポキシ樹脂鋼張り積層板を使用して、(2)直径0.4mmの貫通孔3をドリル加工により設けた。

(3) 該貫通孔3に硬化性導電物質4として、市販の熱硬化性銀ペースト(徳力化研(株)社製、PS-652(商品名))を、その硬化体が貫通孔3より若干突出するようにスクリーン印刷法により充填した。該銀ペーストを熱風乾燥炉で80°Cで4時間、150°Cで2時間の条件で乾燥硬化して導電性を有する充填物4を構成した。(4) 次に320番及び600番のバフを順次使用して、硬化した銀ペーストの硬化体が突出した面を研削し、該硬化体を含む導電層表面を平滑化した。

【0078】次いで、(5)平滑化された導電層表面に、エッティングレジスト17としてドライフィルム(ハイキュレス(株)社製「アクリマーCF」1.5ml)をラミネートし、露光、現像してレジストパターンを形成した。その後、(6)塩化第2銅エッティング液でエッティングを行い、(7)エッティングレジストを剥離することによって、ランド部11を有する第1層配線パターン2、2'を有する両面回路基板5を得た。

【0079】次いで、図7に示すように、(1)上記両面回路基板5を使用して(2)スルーホール部Aを含む第1層配線パターン上に、絶縁層を形成するため、感光性絶縁レジスト(プロピコート5000:商品名、日本ペイント社製)を塗布、乾燥し、露光、現像を行った後熟硬化し、電気的接続を必要とする部分に絶縁層6の開口8を有するパターンを形成した。尚、本実施例は、スルーホール部と第1層回路パターン2'が接続する部分において、スルーホール部Aとその周囲のランド部11が露出するように絶縁層6を形成した態様を示す(図7において左側のスルーホールAの下側部分)。

【0080】次に、(3)上記絶縁層の表面を粗面化処理した後、その両面に無電解メッキ、電解メッキを施し、厚み10μmの銅メッキ層14を形成した。次いで、(4)銅メッキ層14表面に、前記(5)で使用したエッティングレジスト17をラミネートし、露光、現像してレジストパターンを形成し、塩化第2銅エッティング液でエッティングを行った後、エッティングレジストを剥離することによって、配線パターン7、7'を形成して4層の回路パターンを有する多層回路基板を得た。

【0081】得られた多層回路基板について、その表裏に位置し、且つ共通するスルーホールに接続する配線バ

ターン7、7'間の抵抗を測定した結果、33mΩであった。また、図10に示すような、多層回路基板の表裏に位置する該配線パターン7、7'間を含むテストパターンを使用したJIS C-5012の熱衝撃試験（-65°C×30分→125°C30分のサイクル）において、サイクル数500回過ぎても、上記の回路パターン7、7'間を含むテストパターンの導通はあり、また、その後の電気的抵抗の上昇もほとんどなかった。

#### 【0082】実施例3

以下の方法により、銅ペーストよりなる硬化性導電物質を調製した。即ち、平均粒径6.8μm、タップ密度2.99g/cm<sup>3</sup>、比表面積4200cm<sup>2</sup>/gの樹枝状電解銅粉に、リノール酸を銅粉表面に対し、0.25×10<sup>-5</sup>mmol/cm<sup>2</sup>の割合で配合し、窒素雰囲気下で15分間、乳鉢により予備混合した。このようにして得た前処理銅粉を、ネオベンチルグリコールグリジルエーテル（エボキシ当量=150）/ノボラック型フェノール樹脂（ヒドロキシ当量=105）=74/26（重量比）のペインダー100重量部に対し、456重量部添加し、更に、2-エチル-4-メチルイミダゾールを、ペインダー100重量部に対し、2.8重量部添加した後、3本ロールミルで30分間混練してペースト状とした。

【0083】実施例1の方法において、上記銅ペーストを銀ペーストに代えて使用した以外は同様にして多層回路基板の製造を実施した。

【0084】得られた多層回路基板の表裏に位置し、且つ共通するスルーホールに接続する配線パターン7、7'間の抵抗を測定した結果、39mΩであった。また、図10に示すような、多層回路基板の表裏に位置する該配線パターン7、7'間を含むテストパターンを使用したJIS C-5012の熱衝撃試験（-65°C×30分→125°C30分のサイクル）において、サイクル数500回を過ぎても、上記の回路パターン7、7'間を含むテストパターンの導通はあり、その後の電気的抵抗の上昇もほとんどなかった。

#### 【0085】実施例4

実施例1において、スルーホール部を含む平滑化された導電層表面に、図8の（4'）に示す銅メッキ層16を形成しなかった以外は同様にして回路基板を製造した。

【0086】得られた多層回路基板の表裏に位置し、且つ共通するスルーホールに接続する配線パターン7、7'間の抵抗を測定した結果、37mΩであった。また、図10に示すような、多層回路基板の表裏に位置する該配線パターン7、7'間を含むテストパターンを使用したJIS C-5012の熱衝撃試験（-65°C×30分→125°C30分のサイクル）において、サイクル数300回まで上記の多層回路基板の表裏に位置する回路パターン7、7'間を含むテストパターンの導通があったが、その後電気的抵抗の若干の上昇が見られ始

めた。

#### 【図面の簡単な説明】

【図1】本発明の多層回路基板の1つの例を示す断面図である。

【図2】多層回路基板の1つの従来例を示す断面図である。

【図3】多層回路基板の今1つの従来例を示す断面図である。

【図4】多層回路基板の更に今1つの従来例を示す断面図である。

【図5】本発明の多層回路基板の今1つの例を示す断面図である。

【図6】本発明の多層回路基板の製造工程の1例を示す一連の断面図である。

【図7】本発明の多層回路基板の製造工程の今1つの例を示す一連の断面図である。

【図8】図6の製造工程に使用した両面回路基板の製造工程を示す一連の断面図である。

【図9】図7の製造工程に使用した両面回路基板の製造工程を示す一連の断面図である。

【図10】本発明の多層回路基板に対するJIS C-5012に従う熱衝撃試験用のパターンを示す図である。

【図11】片面に3層の回路パターンを有する本発明の多層回路基板を例示する断面図である。

#### 【符号の説明】

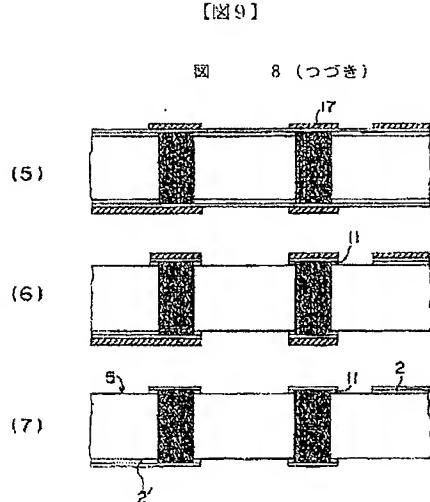
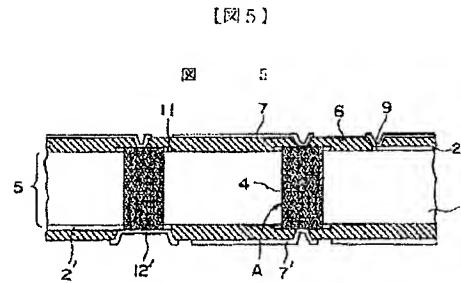
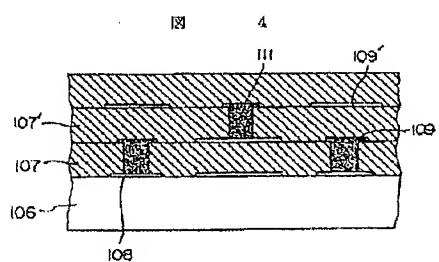
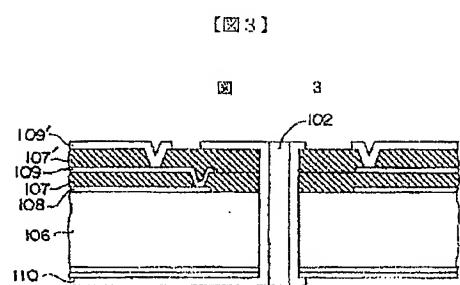
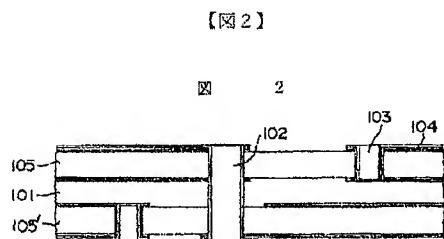
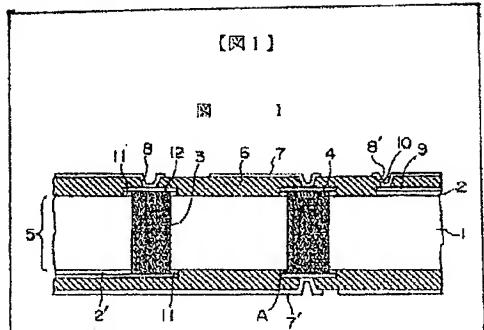
- 1 絶縁基板
- 2 第1層回路パターン
- 2' 第1層回路パターン
- 4 導電性物質
- 5 両面回路基板
- 6 絶縁層
- 7 第2層回路パターン
- 7' 第2層回路パターン
- 8 開口
- 8' 開口
- 9 パターンの端子部
- 10 メッキ層
- 11 ランド部
- 12 メッキ層
- 12' メッキ層
- 13 端子部
- 14 メッキ層
- 15 導電層
- 16 メッキ層
- 17 エッティングレジスト
- 101 プリプレグ
- 102 共通スルーホール
- 103 スルーホール
- 104 回路パターン

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105 両面回路基板  
105' 両面回路基板  
106 絶縁基板  
107 絶縁層

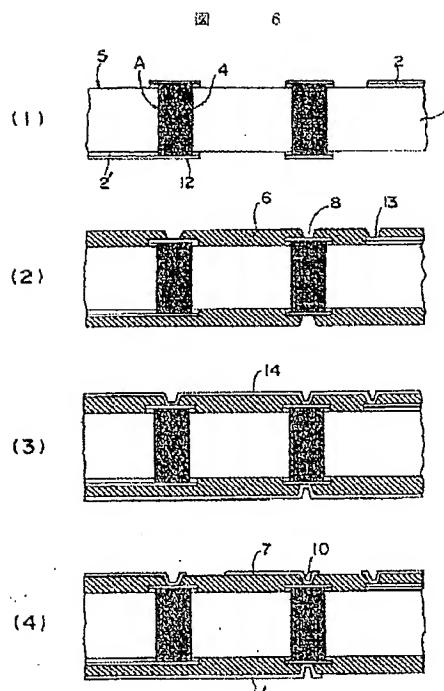
108 第1層回路パターン  
109 第2層回路パターン  
109' 第3層回路パターン



(11)

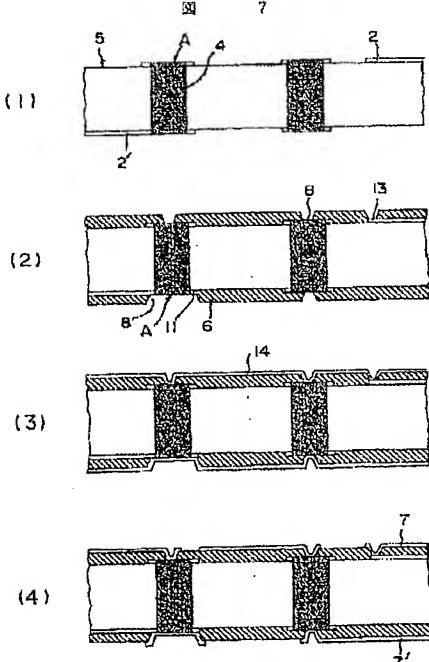
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【図6】



【図11】

【図7】



【図12】

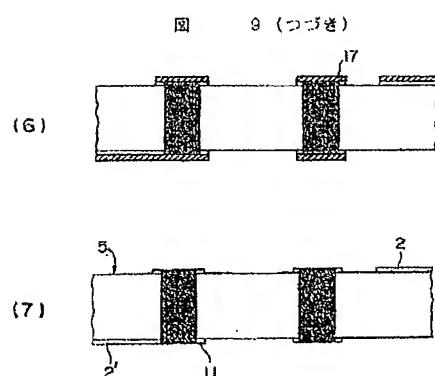
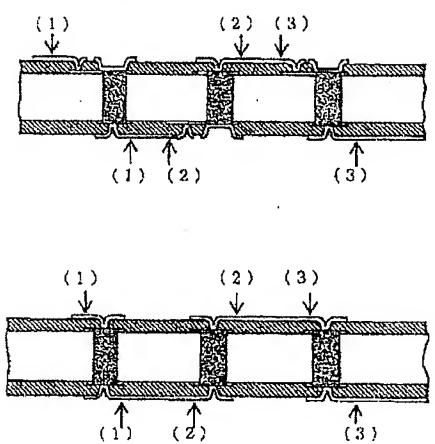


図 10

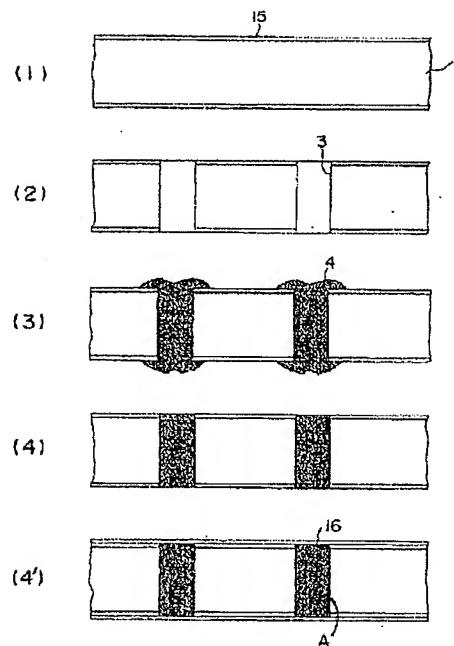


(12)

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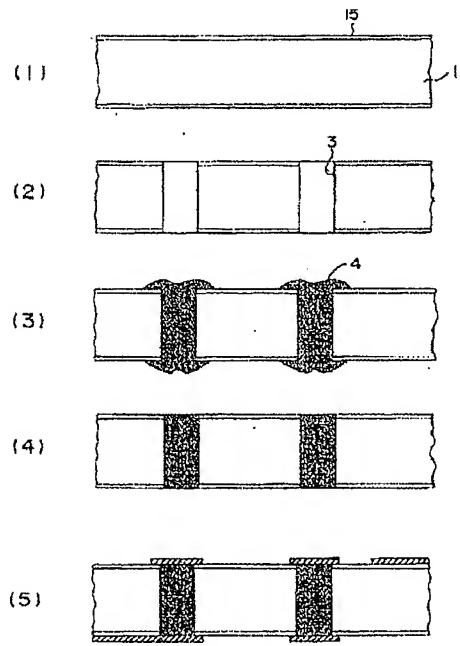
【図8】

図 8



【図10】

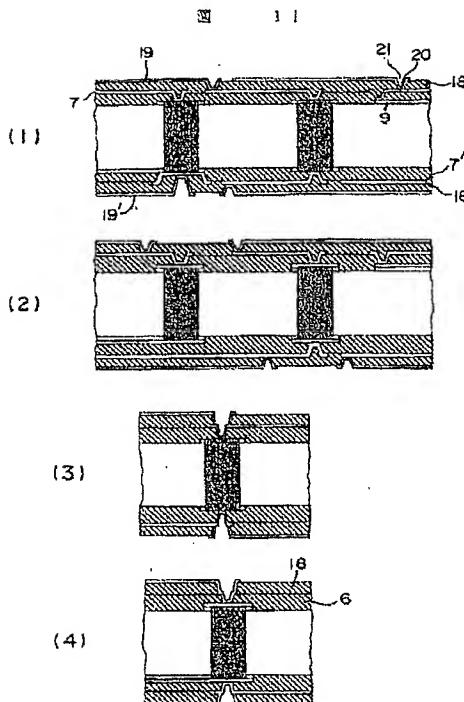
図 9



(13)

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【図13】



## 【手続補正書】

【提出日】平成5年8月2日

【手続補正1】

【補正対象特類名】明細書

【補正対象項目名】図面の簡単な説明

【補正方法】変更

【補正内容】

【図面の簡単な説明】

【図1】本発明の多層回路基板の1つの例を示す断面図である。

【図2】多層回路基板の1つの従来例を示す断面図である。

【図3】多層回路基板の今1つの従来例を示す断面図である。

【図4】多層回路基板の更に今1つの従来例を示す断面図である。

【図5】本発明の多層回路基板の今1つの例を示す断面図である。

【図6】本発明の多層回路基板の製造工程の1例を示す

一連の断面図である。

【図7】本発明の多層回路基板の製造工程の今1つの例を示す一連の断面図である。

【図8】図6の製造工程に使用した両面回路基板の製造工程を示す一連の断面図である。

【図9】図7の製造工程に使用した両面回路基板の製造工程を示す一連の断面図である。

【図10】本発明の多層回路基板に対するJIS C-5012に従う熱衝撃試験用のパターンを示す図である。

【図11】片面に3層の回路パターンを有する本発明の多層回路基板を例示する断面図である。

【図12】本発明の多層回路基板に対するJIS C-5012に従う熱衝撃試験用のパターンを示す図である。

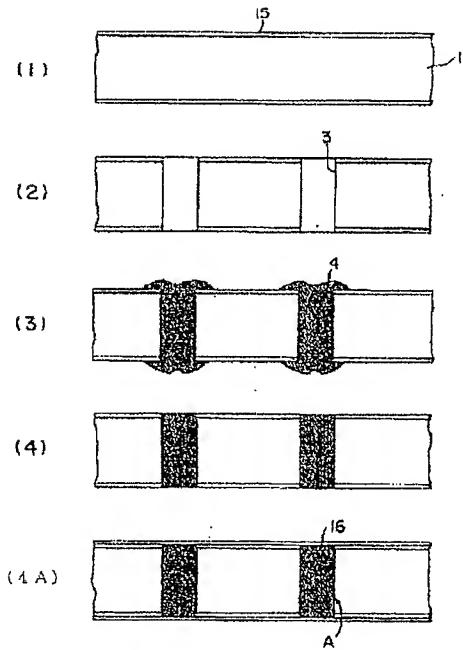
【図13】片面に3層の回路パターンを有する本発明の多層回路基板を例示する断面図である。

【符号の説明】

1 絶縁基板  
 2 第1層回路パターン  
 2' 第1層回路パターン  
 4 導電性物質  
 5 両面回路基板  
 6 絶縁層  
 7 第2層回路パターン  
 7' 第2層回路パターン  
 8 開口  
 8' 開口  
 9 パターンの端子部  
 10 メッキ層  
 11 ランド部  
 12 メッキ層  
 12' メッキ層  
 13 端子部  
 14 メッキ層  
 15 塗電層  
 16 メッキ層  
 17 エッチングレジスト  
 101 プリプレグ  
 102 共通スルーホール  
 103 スルーホール  
 104 回路パターン  
 105 両面回路基板  
 105' 両面回路基板  
 106 絶縁基板  
 107 絶縁層  
 108 第1層回路パターン  
 109 第2層回路パターン  
 109' 第3層回路パターン  
 【手続補正2】  
 【補正対象書類名】図面  
 【補正対象項目名】図8  
 【補正方法】変更  
 【補正内容】  
 【図8】

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図 8



## 【手続補正3】

【補正対象書類名】図面

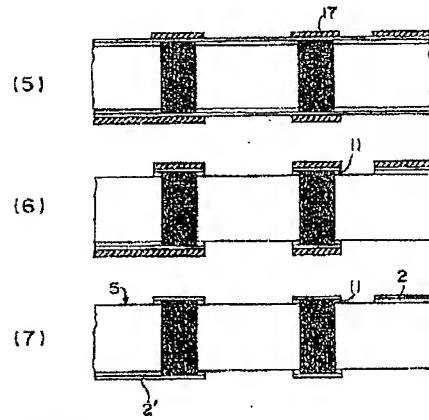
【補正対象項目名】図9

【補正方法】変更

【補正内容】

【図9】

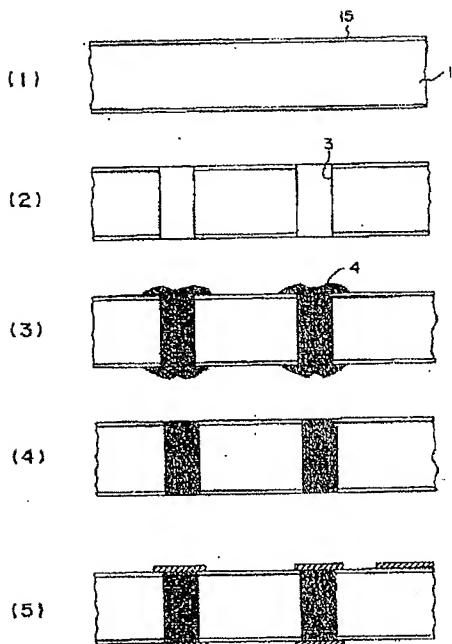
図 9



## 【手続補正4】

【補正対象書類名】図面  
 【補正対象項目名】図10  
 【補正方法】変更  
 【補正内容】  
 【図10】

図 10



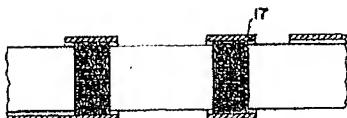
【手続補正5】  
 【補正対象書類名】図面  
 【補正対象項目名】図11  
 【補正方法】変更  
 【補正内容】  
 【図11】

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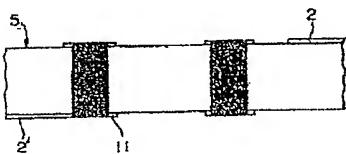
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図 11

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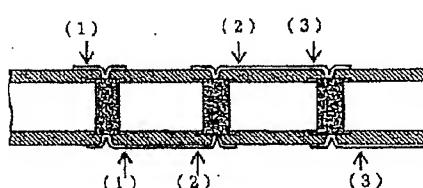
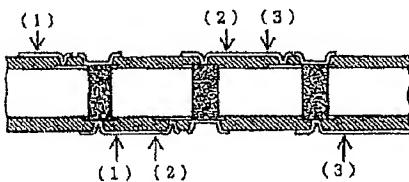


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【手続補正6】  
 【補正対象書類名】図面  
 【補正対象項目名】図12  
 【補正方法】変更  
 【補正内容】  
 【図12】

図 12



【手続補正7】  
 【補正対象書類名】図面  
 【補正対象項目名】図13  
 【補正方法】変更  
 【補正内容】  
 【図13】

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図 13

